MS-16G1 Ver : 0B

Calpella Platform

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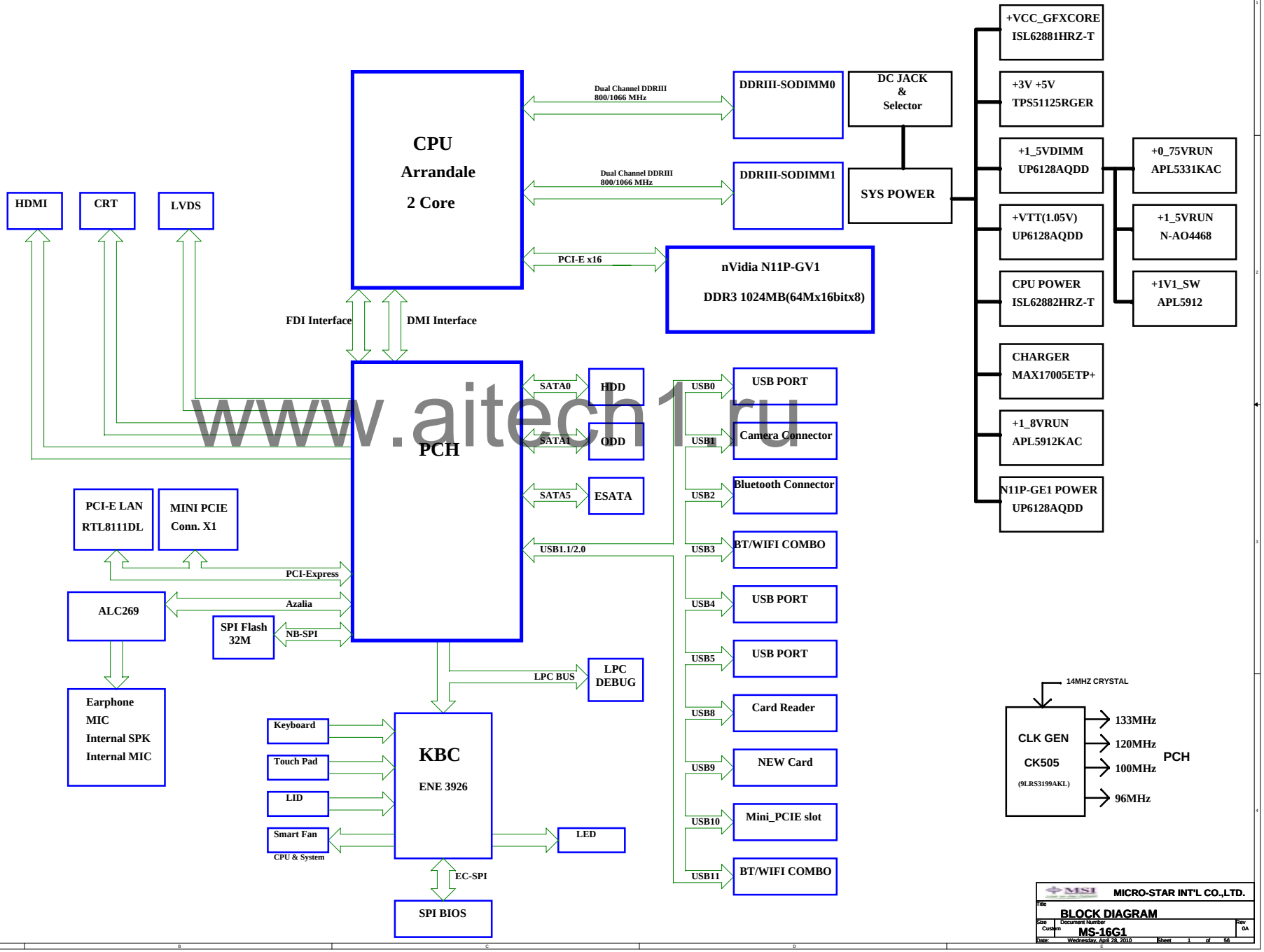


MICRO-STAR INT'L CO.,LTD.

BLOCK DIAGRAM

MS-16G1

Rev 0A

Wednesday, April 28, 2010

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

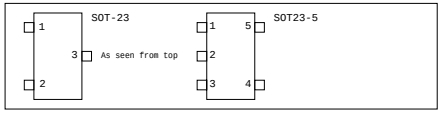
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

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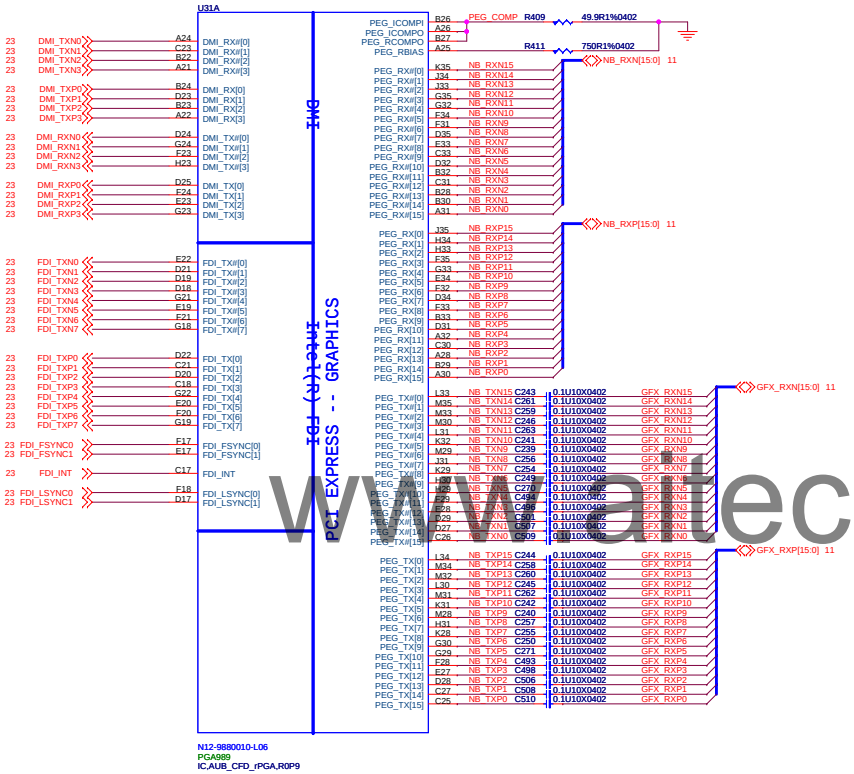
ARRANDALE PROCESSOR (CLK,MISC,JTAG)

10 mils trace wide
20 mils trace space
500 mils trace length

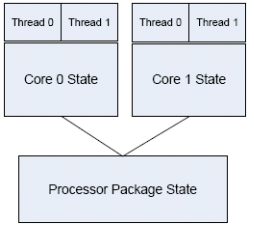


Westmere (formerly Nehalem-C) is the name given to the 32 nm die shrink of Nehalem.

Brand Name	Model (list)	L3 Cache size	Thermal Design Power
Intel Core i3	i3-3xxM	3 MB	35 W
Intel Core i5	i5-4xxM	3 MB	35 W
	i5-5xxM	3 MB	35 W
Intel Core i7	i7-6xxUM	4 MB	18 W
	i7-6xxLM	4 MB	25 W
	i7-6xxM	4 MB	35 W

The Core i3-3xx will be similar to the Core i5-4xx series but running at lower clock speeds and without Turbo Boost

Brand							
Segment	POP1	POP2	POP3	ULV1	ULV2	LV1	LV2
TDP	35W	35W	35W	18W	18W	25W	25W
Cores/ Threads	2/4	2/4	2/4	2/4	2/4	2/4	2/4
CPU Base Freq (GHz)	2.40	2.53	2.66	1.06	1.2	2.00	2.13
Intel® Turbo Boost Technology Max 8C Turbo (GHz)	2.93	3.06	3.33	2.13	2.26	2.80	2.93
DDR3 (MHz)	1066MHz	1066MHz	1066MHz	800MHz	800MHz	1066MHz	1066MHz
L3 Cache	3MB	3MB	4MB	4MB	4MB	4MB	4MB
Integrated Gfx	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Gfx Base Render Frequency	500MHz	500MHz	500MHz	166MHz	166MHz	266MHz	266MHz
Intel® Turbo Boost Technology Max Gfx Render (MHz)	766MHz	766MHz	766MHz	500MHz	500MHz	566MHz	566MHz
Intel® Hyper-threading /VT/TXT/Intel® vPro	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package	BGA/rPGA	BGA/rPGA	BGA/rPGA	BGA	BGA	BGA	BGA



Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1			
		C0	C1	C3	C6
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

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Title: PROCESSOR

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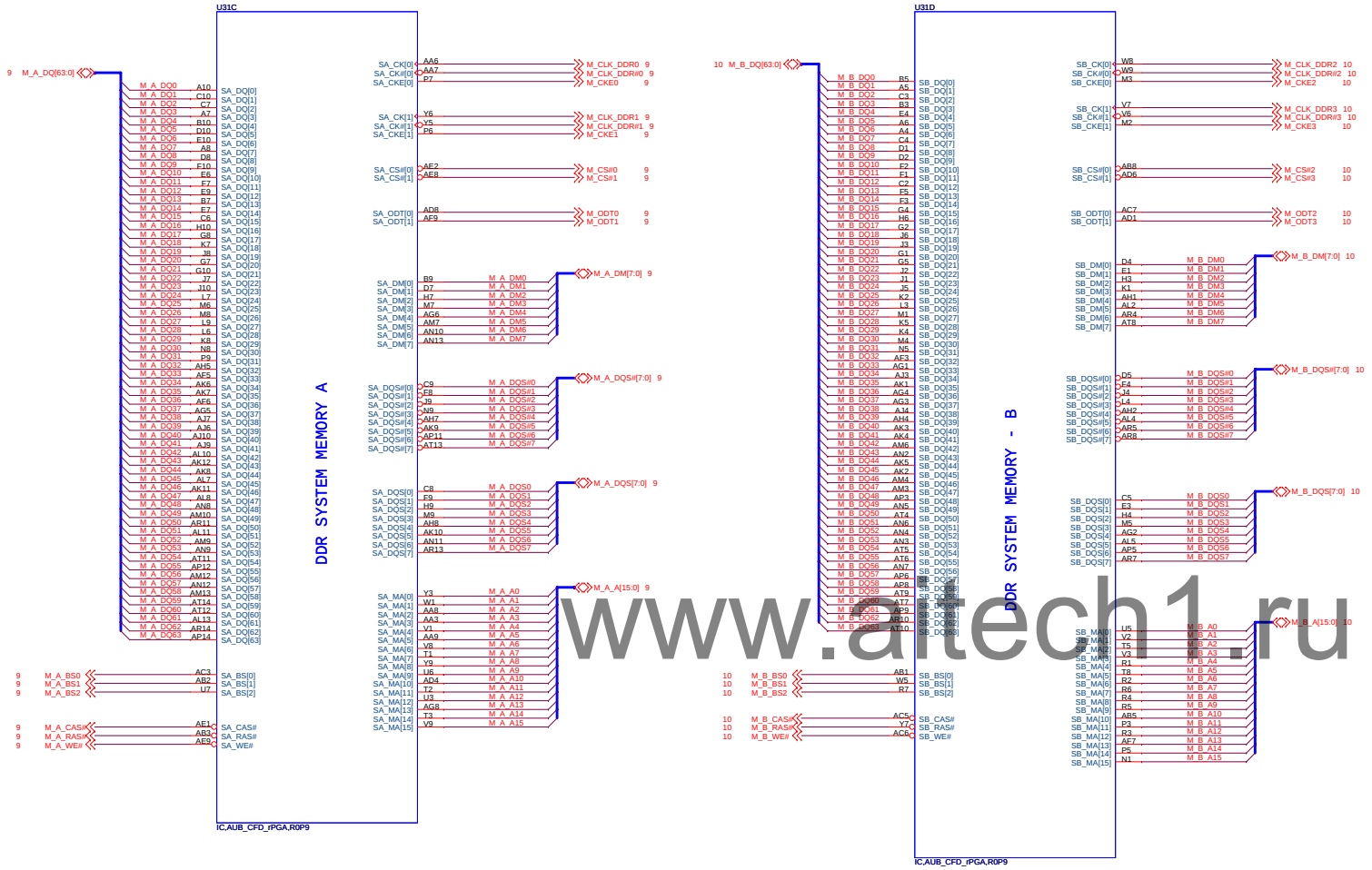
ARRANDALE PROCESSOR (DDR3)



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Title	DDR3		
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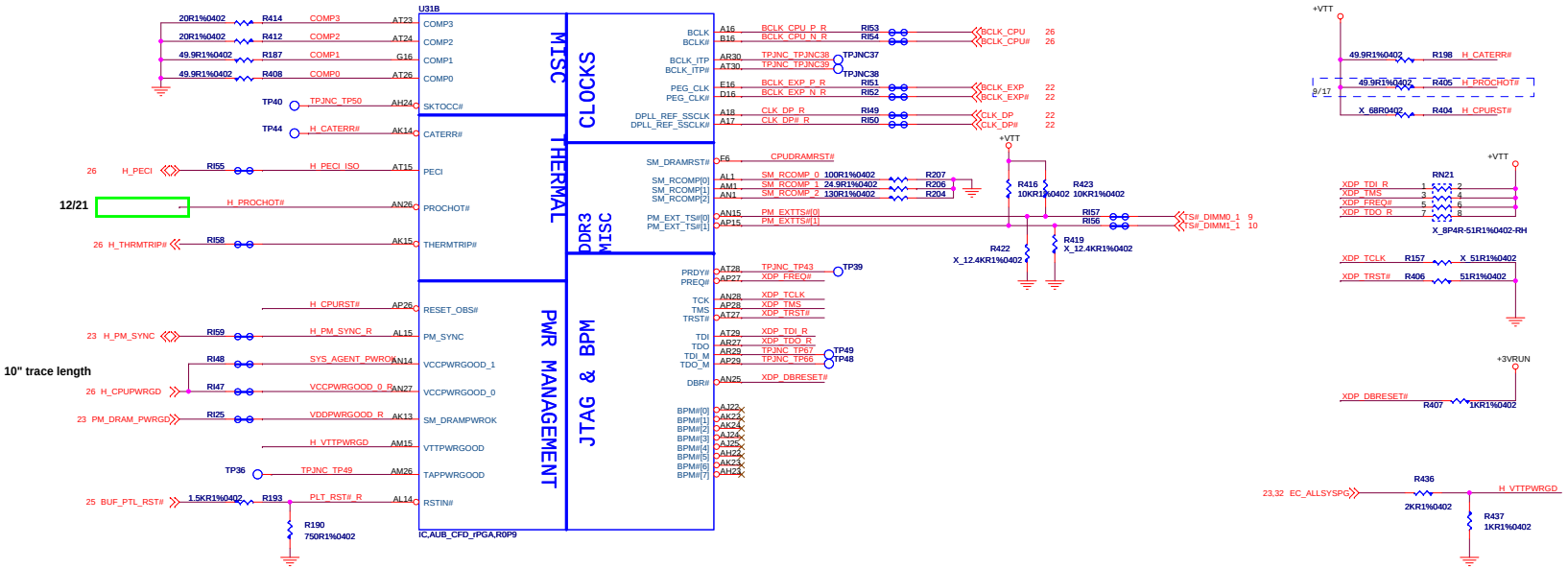
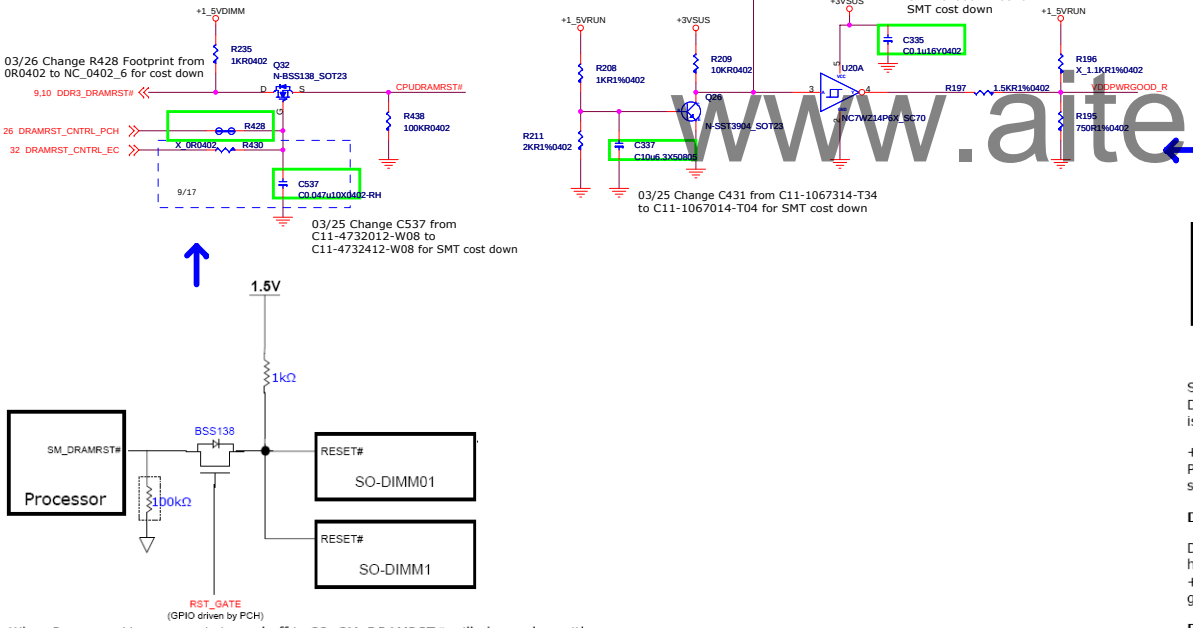
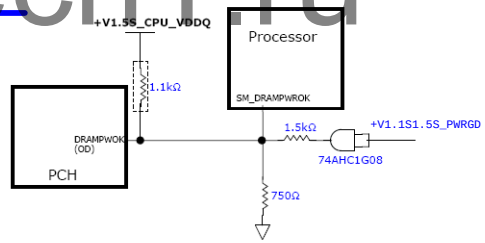




When Processor V_{DDQ} power is turned off in S3, SM_DRAMRST# will also go low with processor power. To avoid SM_DRAMRST# going low, a FET (e.g., BSS138) is added which is controlled using a PCH GPIO (RST_GATE). A Pull-up resistor of 1 kΩ to +1.5V_DIMM is added at SM_DRAMRST#_pin of SO-DIMM. Before system enters S3 (Before SLP_S3# going low), RST_GATE is driven low and FET is turned off. With a 1-kΩ PU on the SO-DIMM side, SM_DRAMRST# is maintained high during S3. When exiting S3, the FET will remain off until the integrated memory controller is reinitialized to drive the SM_DRAMRST# signal to a high level after the Processor V_{DDQ} power is restored.



SM_DRAMPWROK signal is driven low when PROCESSOR is turned off in S3 entry. During S3 exit, this signal is driven high only after +V1.5S_CPU_VDDQ stable. There is no timing requirement between and 0.75-V V_{TT} rail.

+V1.1S1.5S_PWRGD signal is an open-drain signal driven from +V1.5S_CPU_VDDQ PWRGOOD logic. It should go high only after +V1.5S_CPU_VDDQ to processor is stable.

DRAMPWROK behavior in S5/S4 to S0:

During S5/S4 to S0, DRAMPWROK is driven low by PCH until PCH_PWROK becomes high provided SLP_S4# is high. Even though DRAMPWROK derived from PWRGOOD of +V1.5S_CPU_VDDQ comparator, it is overdriven to low by PCH until PCH_PWROK goes high. This implementation ensures that S5 to S0 timings are maintained.

DRAMPWROK behavior in S0 to S3:

This signal is driven low as the +V1.1S1.5S_PWRGD becomes low when +V1.5S_CPU_VDDQ ramps down. To maintain this signal low, this AND gate is powered using SUS rail (+V3.3A). Any buffer/AND gate of 4 mA should work fine in the given circuit.

DRAMPWROK behavior in S3 to S0:

This signal is driven high when +V1.5S_CPU_VDDQ to the processor is stable

DRAMPWROK is 1.1-V/1.05-V signal to processor; hence a resistor divider is implemented to level translate the signal.

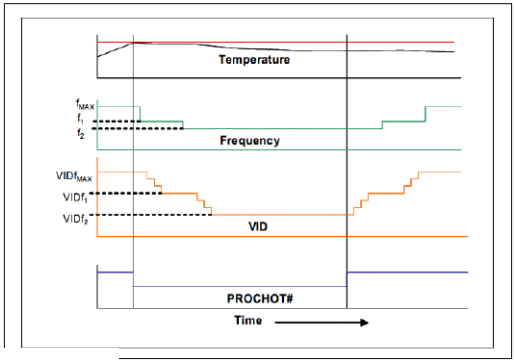
Refer to the latest Intel CRB schematics for more details on +V1.1S1.5S_PWRGD generation.

Arrandale Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory/Graphics
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI/Intel® FDI
DPLL_REF_SSCLK/DPLL_REF_SSCLK#	120 MHz	Embedded DisplayPort (eDP)

Signal Name	Description	Direction/Buffer Type
VCCPWRGOOD_0 VCCPWRGOOD_1	**VCCPWRGOOD_0 and VCCPWRGOOD_1 (Power Good) Processor Input:** The processor requires these signals to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. Both signals must then transition monotonically to a high state. VCCPWRGOOD_0 and VCCPWRGOOD_1 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of these signals. VCCPWRGOOD_0 and VCCPWRGOOD_1 should be tied together and connected to the PROCPWRGD output signal of the PCH.	I Asynchronous CMOS

Frequency and Voltage Ordering



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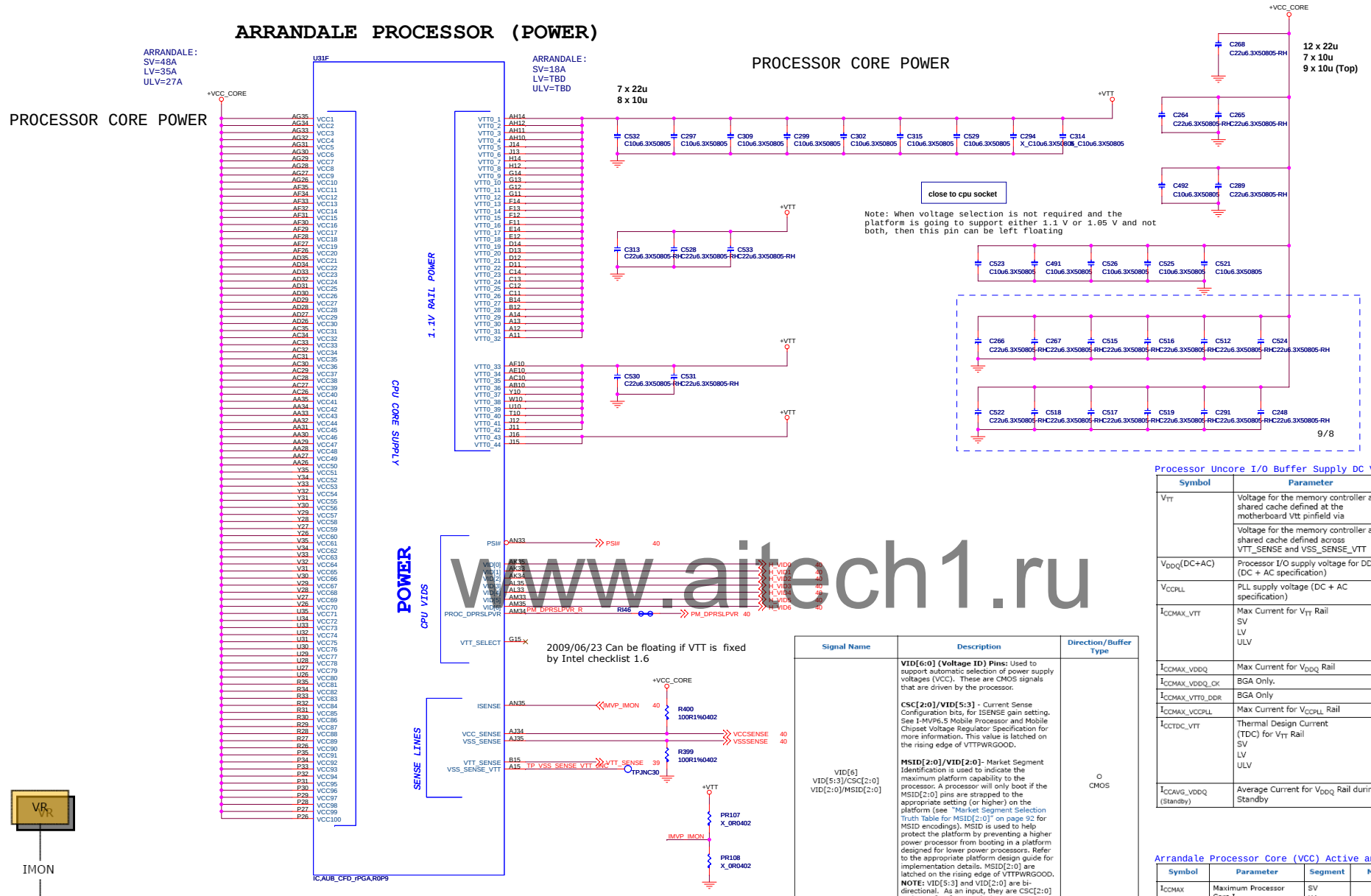
ARRANDALE PROCESSOR (POWER)



Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{TT}	Voltage for the memory controller and shared cache defined at the motherboard Vtt pinfield via	0.9975	1.05	1.1025	V
	Voltage for the memory controller and shared cache defined across VTT_SENSE and VSS_SENSE_VTT	0.9765	1.05	1.1235	V
V_{DDQ}(DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	1.425	1.5	1.575	V
V_{CCPLL}	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V
I_{CCMAX_VTT}	Max Current for V_{TT} Rail SV LV ULV		-	 18 16 16	A
I_{CCMAX_VDDQ}	Max Current for V_{DDQ} Rail		-	3	A
$I_{CCMAX\_VDDQ\_CK}$	BGA Only.			0.2	A
$I_{CCMAX\_VTT0\_DDR}$	BGA Only			2.6	A
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail		-	1.35	A
I_{CCTDC_VTT}	Thermal Design Current (TDC) for V_{TT} Rail SV LV ULV		-	 18 16 16	A
I_{CCAVG_VDDQ} (Standby)	Average Current for V_{DDQ} Rail during Standby		-	0.33	A

Signal Name	Description	Direction/Buffer Type
VID[6] VID[5:3]/CSC[2:0] VID[2:0]/MSID[2:0]	**VID[6:0] (Voltage ID) Pins:** Used to support automatic selection of power supply voltages (VCC). These are CMOS signals that are driven by the processor. **CSC[2:0]/VID[5:3]** - Current Sense Configuration bits, for ISENSE gain setting. See I-MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulator Specification for more information. This value is latched on the rising edge of VTTPWRGOOD. **MSID[2:0]/VID[2:0]**- Market Segment Identification is used to indicate the maximum platform capability to the processor. A processor will only boot if the MSID[2:0] pins are strapped to the appropriate setting (or higher) on the platform (see "Market Segment Selection Truth Table for MSID[2:0]" on page 92 for MSID encodings). MSID is used to help protect the platform by preventing a higher power processor from booting in a platform designed for lower power processors. Refer to the appropriate platform design guide for implementation details. MSID[2:0] are latched on the rising edge of VTTPWRGOOD. **NOTE:** VID[5:3] and VID[2:0] are bi-directional. As an input, they are CSC[2:0] and MSID[2:0] respectively.	O CMOS

Arrandale Processor Core (VCC) Active and Idle Mode DC Voltage and Current

Symbol	Parameter	Segment	Min	Typ	Max	Unit
I_{CCMAX}	Maximum Processor Core I_{CC}	SV LV ULV			48 35 27	A
I_{CC_TDC}	Thermal Design I_{CC}	SV LV ULV			32 22 16	A
I_{CC_LFM}	I_{CC} at LFM	SV LV ULV			18 12 8	A
I_{C6}	I_{CC} at C6 Idle-state	SV LV ULV			0.3 0.3 0.3	A

Table 17. IA Core I_{MAX} and Gain Definition – Defined Relative to CPU Core Maximum Current

CPU SKU, $I_{CC\_CORE-MAX}$ Maximum CPU Core Current	I_{MAX} (IMON=900 mV min) [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
$I_{CC\_CORE-MAX}$ ≤20 A	20	001	45.0
20A< $I_{CC\_CORE-MAX}$ ≤30 A	30	010	30.0
30A< $I_{CC\_CORE-MAX}$ ≤40 A	40	011	22.5
40A< $I_{CC\_CORE-MAX}$ ≤50 A	50	100	18.0
50A< $I_{CC\_CORE-MAX}$ ≤60 A	60	101	15.0
60A< $I_{CC\_CORE-MAX}$ ≤70 A	70	110	12.9
70A< $I_{CC\_CORE-MAX}$ ≤90 A	90	111	10.0

Table 43. Market Segment Selection Truth Table for MSID[2:0]

MSID[2]	MSID[1]	MSID[0]	Description[1,2]
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Arrandale Standard Voltage (SV) 35W Supported
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

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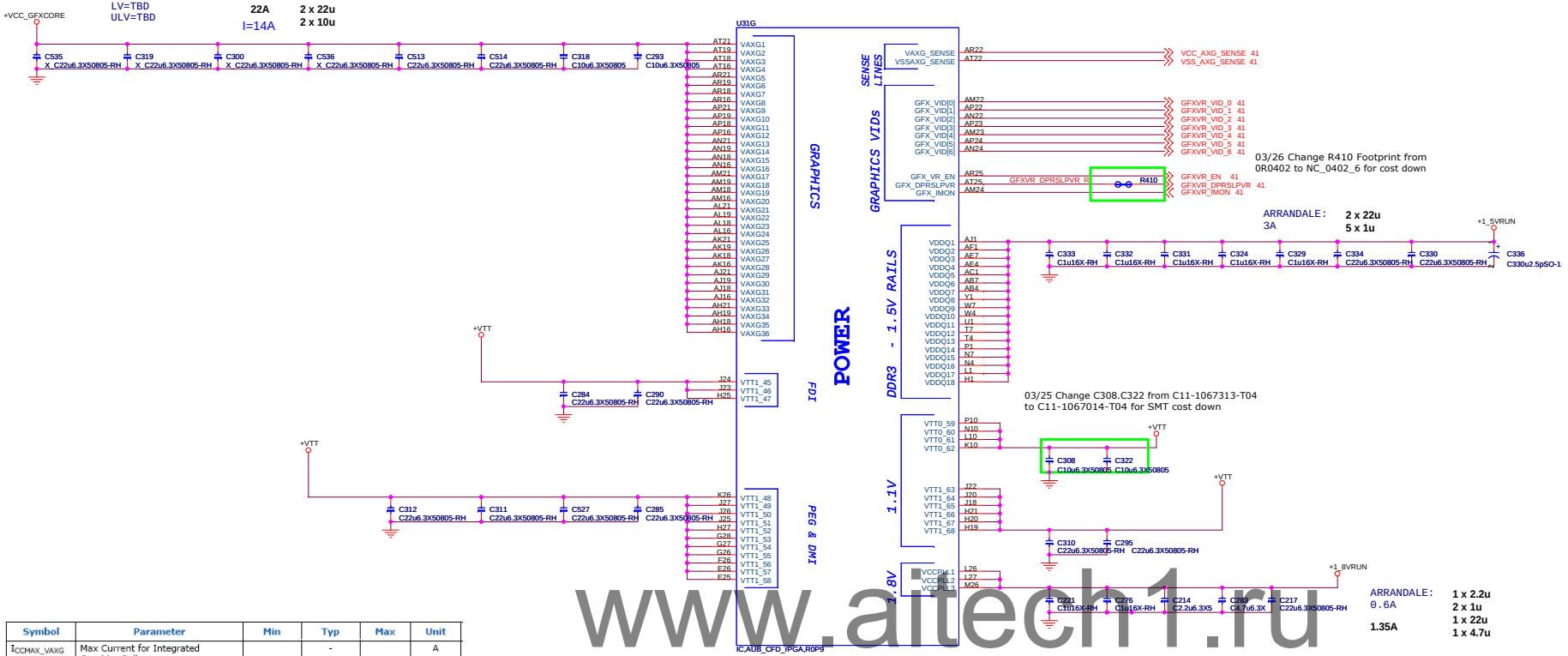
ARRANDALE PROCESSOR (GRAPHICS POWER)

ARRANDALE:
SV=15A
LV=TBD
ULV=TBD

22A
I=14A

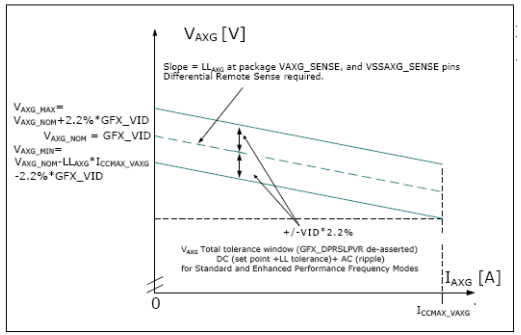
2 x 22u
2 x 10u



Symbol	Parameter	Min	Typ	Max	Unit
I_{CCMAX_VAXG}	Max Current for Integrated Graphics Rail SV LV ULV		-	 22 15 12	A
I_{CCTDC_VAXG}	Thermal Design Current (TDC) for Integrated Graphics Rail SV LV ULV		-	 12 7 6	A

Symbol	Parameter	Min	Typ	Max	Unit
V_{AXG}	Graphics core voltage		See Figure 15		

V_{AXG}/I_{AXG} Static and Ripple Voltage Regulation



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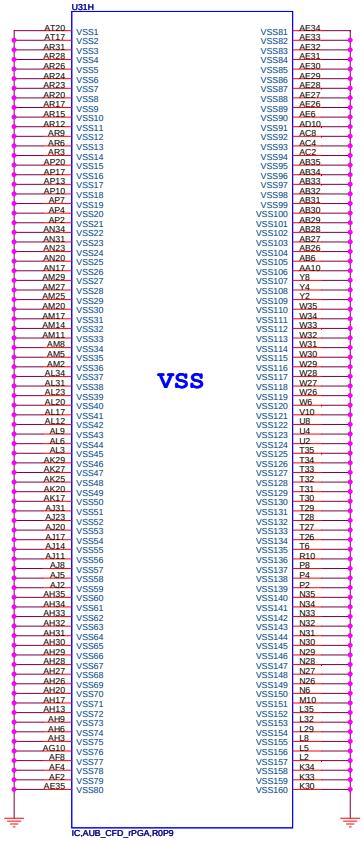
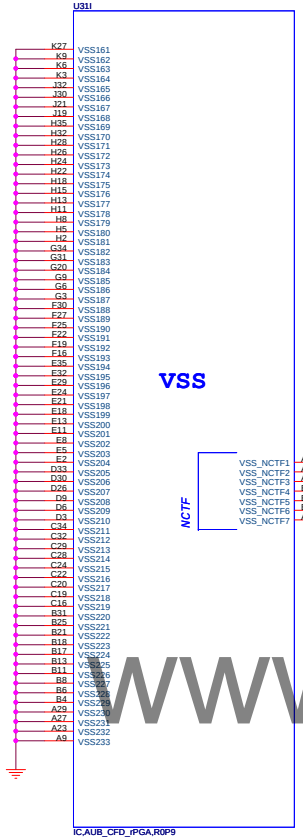
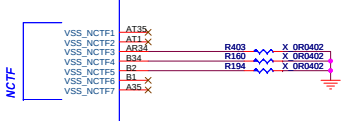
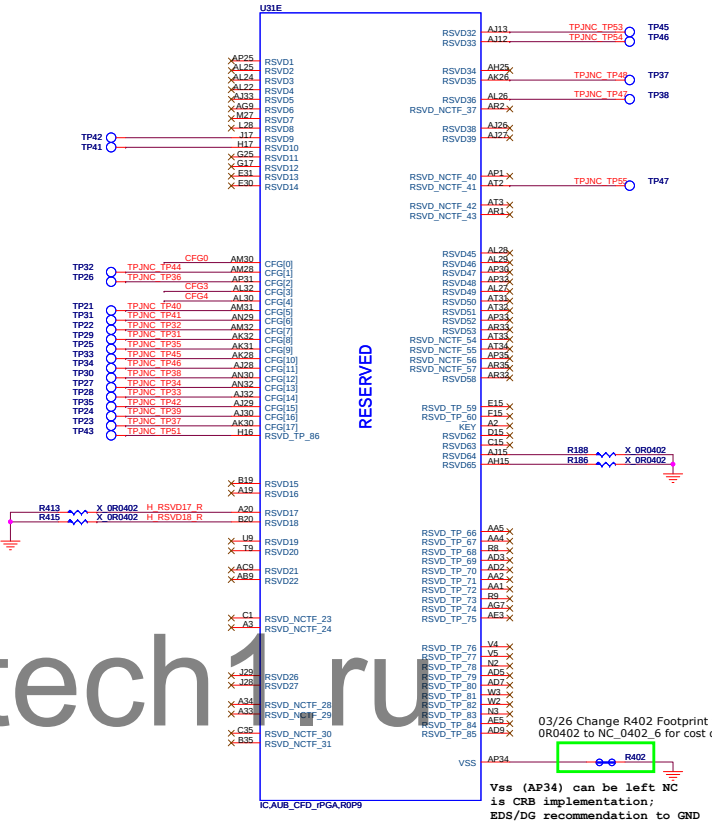
ARRANDALE PROCESSOR (GND)







ARRANDALE PROCESSOR (RESERVED)



03/26 Change R402 Footprint from 0R0402 to NC_0402_6 for cost down

Vss (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

Processor Core/Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C1E	AutoHALT state with lowest frequency and voltage operating point.
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.

DMI States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

Integrated Memory Controller States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed.
Active Power down	CKE deasserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE deasserted using device self-refresh.

Integrated Graphics Controller States

State	Description
D0	Full on, display active.
D3 Cold	Power-off.

PCIe Link States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG0 — NO_STUFF R159 X_3.01KR1%0402

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG3 — STUFF R158 3.01KR1%0402

CFG[3] PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
1: No lane reversal
0: Reversal

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 — NO_STUFF R156 X_3.01KR1%0402

Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

MICRO-STAR INT'L CO.,LTD.

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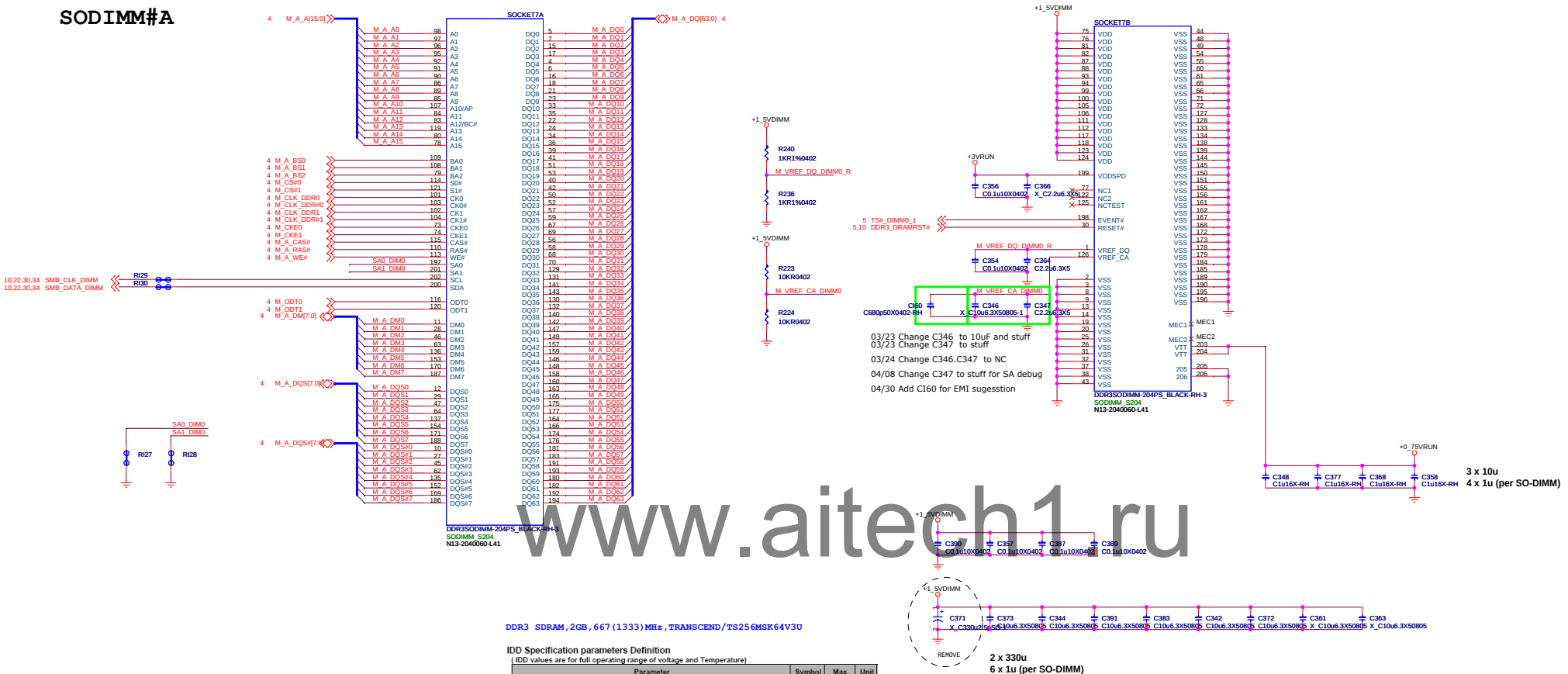
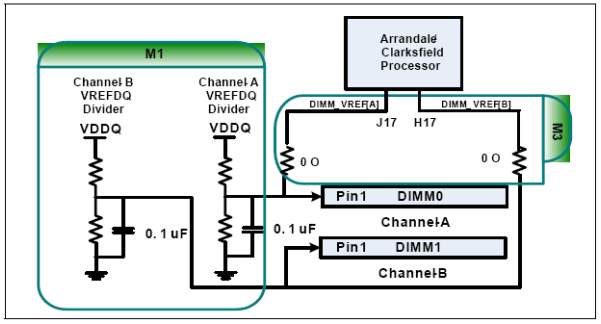


2.5.4 DDR3 VREFDQ Design Implementation

Intel is requesting that customers implement two methods (M1 and M3) to generate and control the DDR3 SO-DIMM Reference voltage for Data/Strobe inputs (V_{REFDQ}) on Arrandale- and Clarksfield-based platforms. For Arrandale, M1 should be used. For Clarksfield only designs and common motherboard designs (which support both Arrandale and Clarksfield processors), both M1 and M3 methods should be con-currently implemented.

Note: DDR3 V_{REFDQ} recommendation outlined above in this document, V_{REFCA} and V_{REFDQ} on SO-DIMM cannot be tied together any more for Clarksfield only and Common motherboard designs in order to support M3 and M1/M3 co-existence.

Figure 33. Clarksfield DDR3 SO-DIMM VREF_DQ Design Requirements



IDD Specification parameters Definition
(IDD values are for full operating range of voltage and Temperature)

Parameter	Symbol	Max.	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1,200	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	1,360	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	800	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	960	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	960	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	800	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	1,000	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	2,120	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	2,320	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	2,240	mA
Self refresh current; CK and /CKat 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R	IDD7	3,400	mA

MSI	MICRO-STAR INT'L CO.,LTD.
Title	DDR3 SODIMM0
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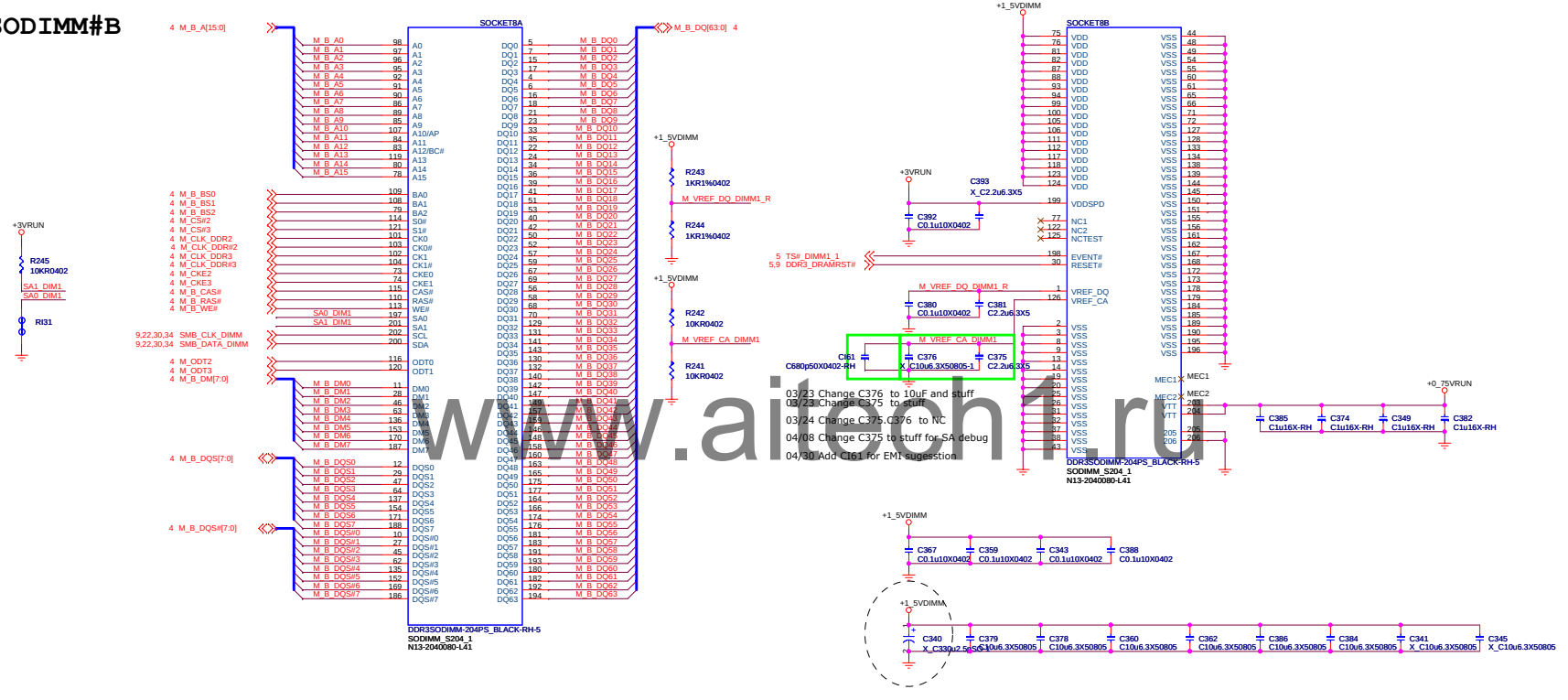
SODIMM#B



03/23 Change C376 to 10uF and stuff
03/23 Change C375 to stuff
03/24 Change C375,C376 to NC
04/08 Change C375 to stuff for SA debug
04/30 Add C161 for EMI sugesstion

Title	DDR3 SODIMM1
Company	MICRO-STAR INT'L CO.,LTD.
Size	Custom
Document Number	MS-16G1
Rev	0A
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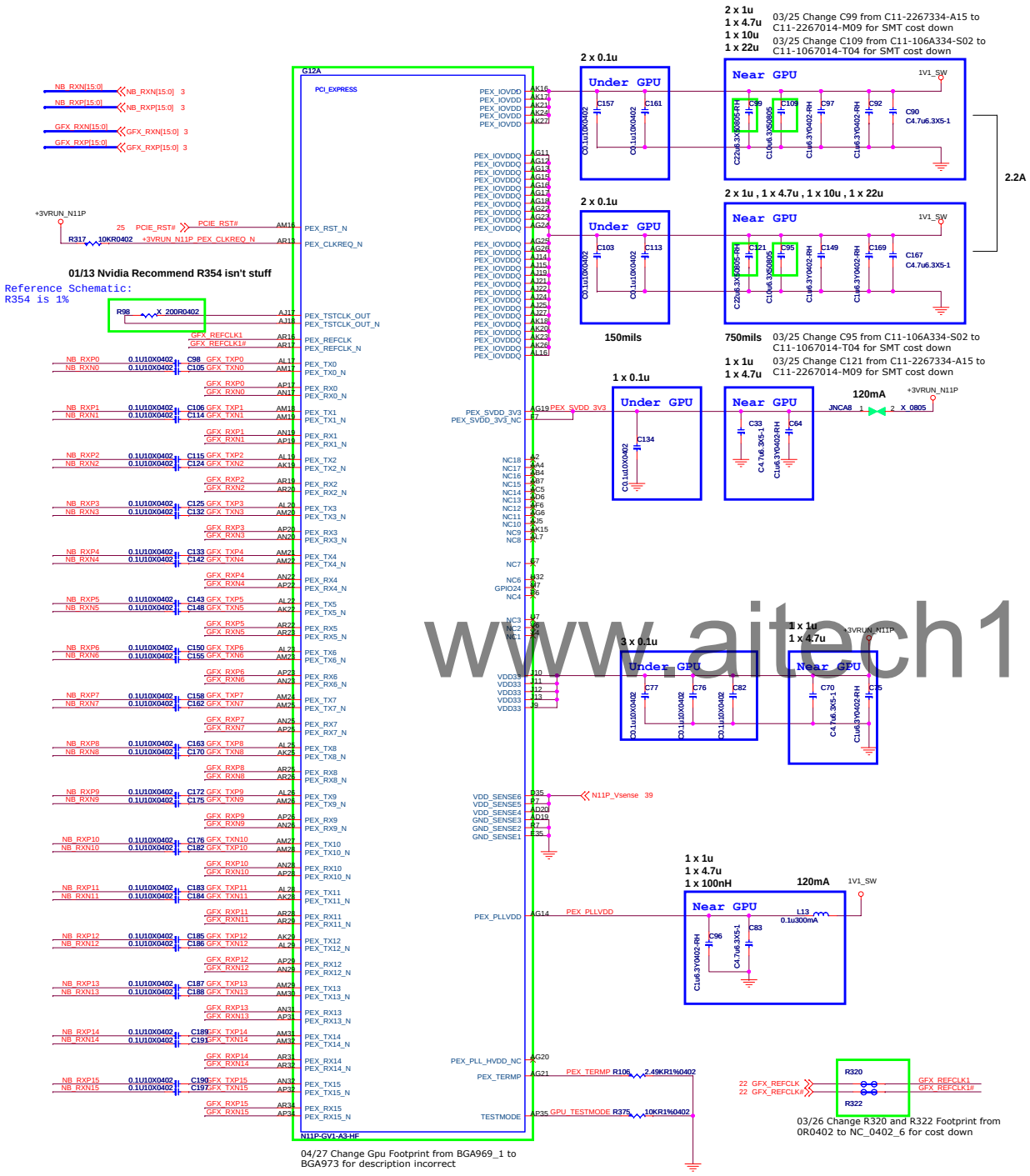


Optimus Software Design for Arrandale Platforms

At POST, the system BIOS should initialize the IGP as the primary graphics adapter. As the OS initializes, both the IGP driver and GPU driver will load. Up to this point the platform is similar to any multiple graphics adapter system-such as a desktop system with more than one graphics card installed. However, the GPU in an Optimus system typically has no physical display outputs. It is purely a graphics rendering and compute device. Then Optimus software will determine when the GPU's capabilities are needed and will enable the GPU as needed, and will host work for individual applications on the GPU as needed.

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_TX	90DIFF	1
PEX_TX	90DIFF	1

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_RX	90DIFF	1
PEX_RX	90DIFF	1

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_CLK_OUT	90DIFF	1
PEX_CLK_OUT	90DIFF	1

SOURCE POWER NETS

NET	MIN_LINE_WIDTH	MAX_CURRENT	VOLTAGE	NV_SOURCE POWER_NET
3V3	16.00	4A	3.30000V	TRUE
12V	25.00	8A	18.00000V	TRUE

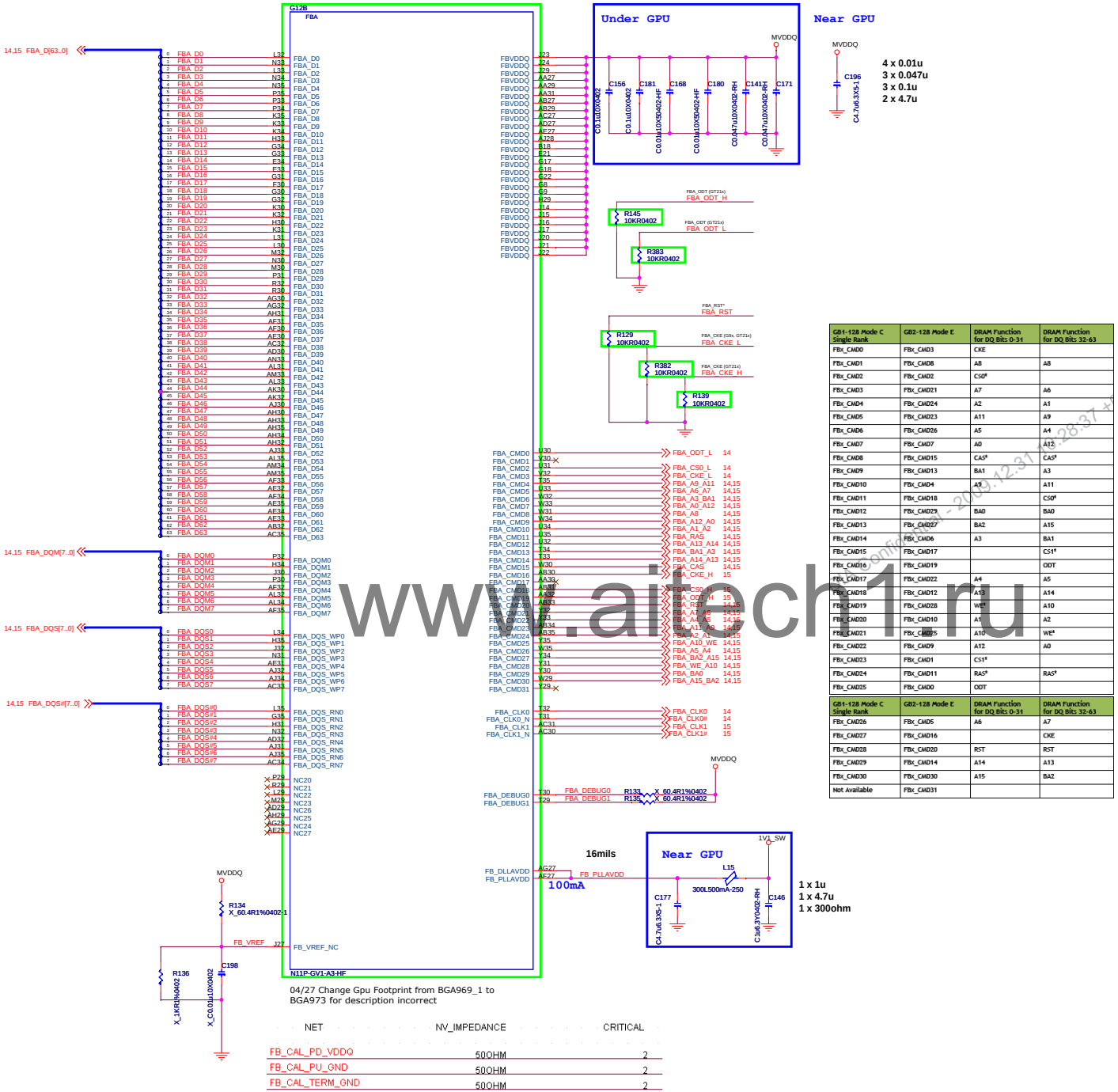
Features	N11P-GE1	N11P-LP1	N11P-GS1
Host Platform	PCIE 2.0 x 16		
Memory Interface	128-bit DDR3 GDDR3		128-bit DDR3 GDDR3 GDDR5
Process Technology	40nm		
Device ID	0x0A29	0x0A2B	0x0CAF
Package	969-ball BGA 29nm x 29nm package BG1-128		
Display	DVII DVID 1920 x1200 @ 60Hz		DVII DVID 2560 x 1600 @ 60Hz

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1 PCIE Host

Size: Custom | Document Number: MS-16G1 | Rev: 0A

Date: Tuesday, May 04, 2010 | Sheet 11 of 56



NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2

GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD0	FBx_CMD3	CKE	
FBx_CMD1	FBx_CMD8	A8	A8
FBx_CMD2	FBx_CMD2	CS0#	
FBx_CMD3	FBx_CMD21	A7	A6
FBx_CMD4	FBx_CMD24	A2	A1
FBx_CMD5	FBx_CMD23	A11	A9
FBx_CMD6	FBx_CMD26	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD8	FBx_CMD15	CAS#	CAS#
FBx_CMD9	FBx_CMD13	BA1	A3
FBx_CMD10	FBx_CMD4	A9	A11
FBx_CMD11	FBx_CMD18		CS0#
FBx_CMD12	FBx_CMD29	BA0	BA0
FBx_CMD13	FBx_CMD27	BA2	A15
FBx_CMD14	FBx_CMD6	A3	BA1
FBx_CMD15	FBx_CMD17		CS1#
FBx_CMD16	FBx_CMD19		ODT
FBx_CMD17	FBx_CMD22	A4	A5
FBx_CMD18	FBx_CMD12	A13	A14
FBx_CMD19	FBx_CMD28	WE#	A10
FBx_CMD20	FBx_CMD10	A1	A2
FBx_CMD21	FBx_CMD25	A10	WE#
FBx_CMD22	FBx_CMD9	A12	A0
FBx_CMD23	FBx_CMD1	CS1#	
FBx_CMD24	FBx_CMD11	RAS#	RAS#
FBx_CMD25	FBx_CMD0	ODT	

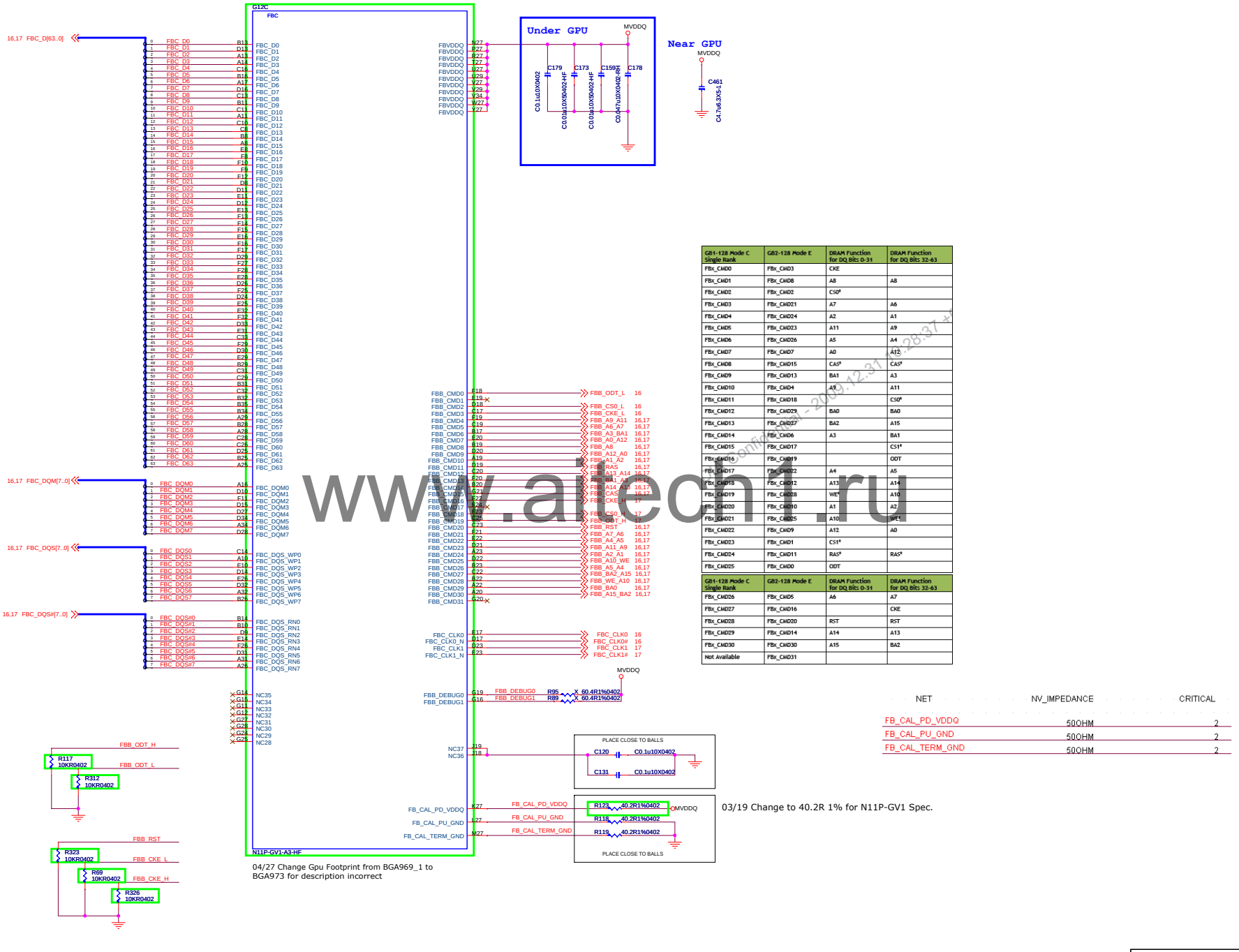
GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD26	FBx_CMD5	A6	A7
FBx_CMD27	FBx_CMD16		CKE
FBx_CMD28	FBx_CMD20	RST	RST
FBx_CMD29	FBx_CMD14	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
Not Available	FBx_CMD31		

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1 MEM Interface A

Size: Custom | Document Number: MS-16G1 | Rev: 0A

Date: Tuesday, May 04, 2010 | Sheet 12 of 56



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD0	FBx_CMD3	CKE	
FBx_CMD1	FBx_CMD8	A8	A8
FBx_CMD2	FBx_CMD2	CS0#	
FBx_CMD3	FBx_CMD21	A7	A6
FBx_CMD4	FBx_CMD24	A2	A1
FBx_CMD5	FBx_CMD23	A11	A9
FBx_CMD6	FBx_CMD26	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD8	FBx_CMD15	CAS#	CAS#
FBx_CMD9	FBx_CMD13	BA1	A3
FBx_CMD10	FBx_CMD4	A9	A11
FBx_CMD11	FBx_CMD18		CS0#
FBx_CMD12	FBx_CMD29	BA0	BA0
FBx_CMD13	FBx_CMD27	BA2	A15
FBx_CMD14	FBx_CMD6	A3	BA1
FBx_CMD15	FBx_CMD17		CS1#
FBx_CMD16	FBx_CMD19		ODT
FBx_CMD17	FBx_CMD22	A4	A5
FBx_CMD18	FBx_CMD12	A13	A14
FBx_CMD19	FBx_CMD28	WE#	A10
FBx_CMD20	FBx_CMD10	A1	A2
FBx_CMD21	FBx_CMD25	A10	WE#
FBx_CMD22	FBx_CMD9	A12	A0
FBx_CMD23	FBx_CMD1	CS1#	
FBx_CMD24	FBx_CMD11	RAS#	RAS#
FBx_CMD25	FBx_CMD0	ODT	

GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FBx_CMD26	FBx_CMD5	A6	A7
FBx_CMD27	FBx_CMD16		CKE
FBx_CMD28	FBx_CMD20	RST	RST
FBx_CMD29	FBx_CMD14	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
Not Available	FBx_CMD31		

NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2

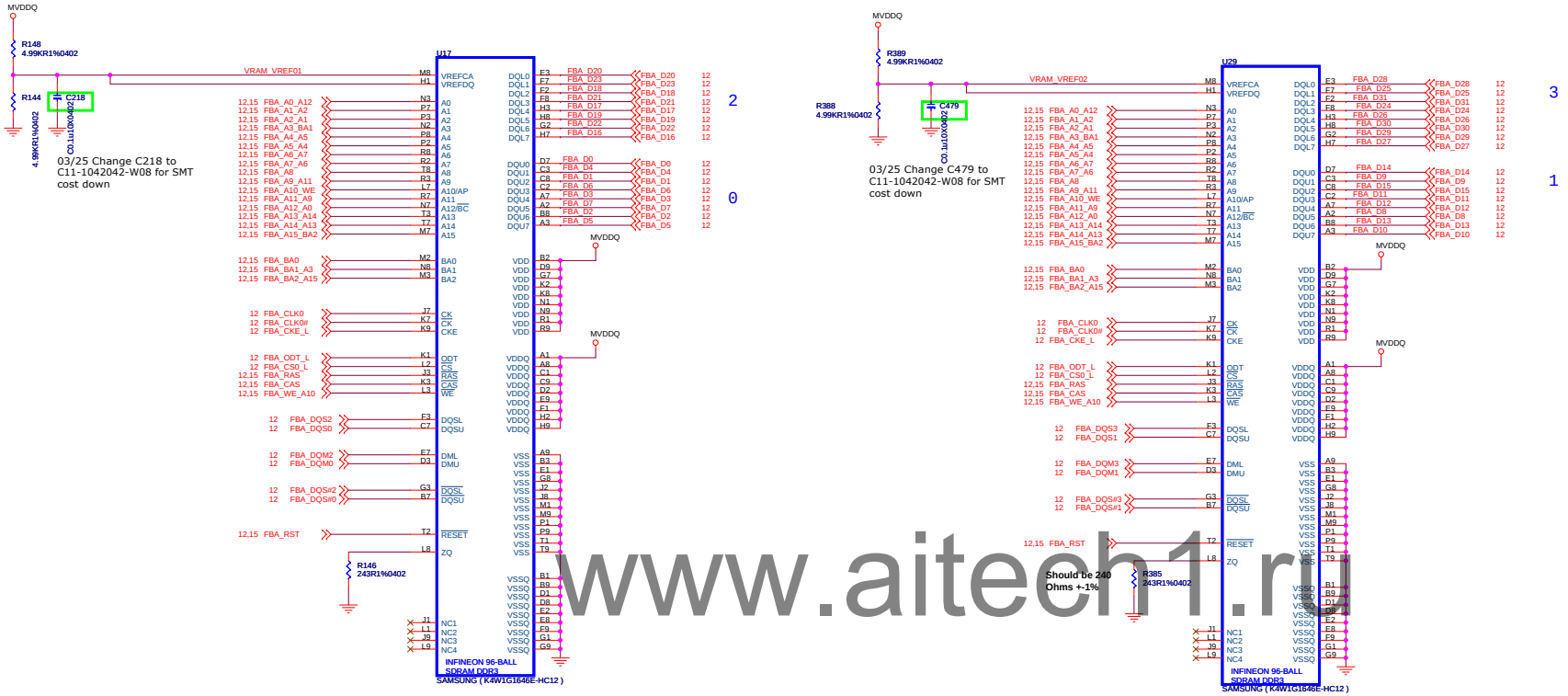
03/19 Change to 40.2R 1% for N11P-GV1 Spec.

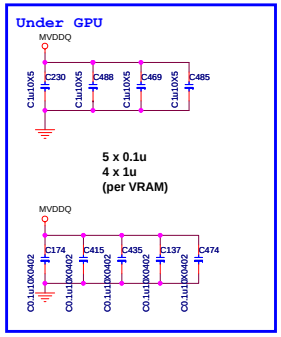
MICRO-STAR INT'L CO.,LTD.

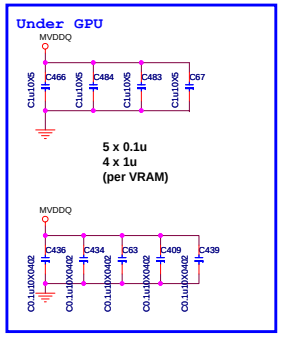
Title: N11P-GV1 MEM Interface B

Size: Custom | Document Number: MS-16G1 | Rev: 0A

Date: Tuesday, May 04, 2010 | Sheet 13 of 56







11.0 1Gb gDDR3 SDRAM E-die IDD Spec Table

[Table 44] IDD Specification for 1Gb gDDR3 E-die

Symbol	64Mx16 (K4W1G1646E)					Unit
	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	
	7-7-7	9-9-9	11-11-11	12-12-12	13-13-13	
IDD0	65	70	80	TBD	TBD	mA
IDD1	85	90	105	TBD	TBD	mA
IDD2P-F	25	25	25	TBD	TBD	mA
IDD2P-S	10	10	10	TBD	TBD	mA
IDD2N	30	35	35	TBD	TBD	mA
IDD2Q	30	35	35	TBD	TBD	mA
IDD3P-F	25	27	30	TBD	TBD	mA
IDD3N	45	50	55	TBD	TBD	mA
IDD4R	130	160	200	TBD	TBD	mA
IDD4W	130	155	195	TBD	TBD	mA
IDD5	150	160	160	TBD	TBD	mA
IDD6	10	10	10	TBD	TBD	mA
IDD7	200	240	290	TBD	TBD	mA

NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1 FrameA DDR3 I

Size: Custom | Document Number: MS-16G1 | Rev: 1.0

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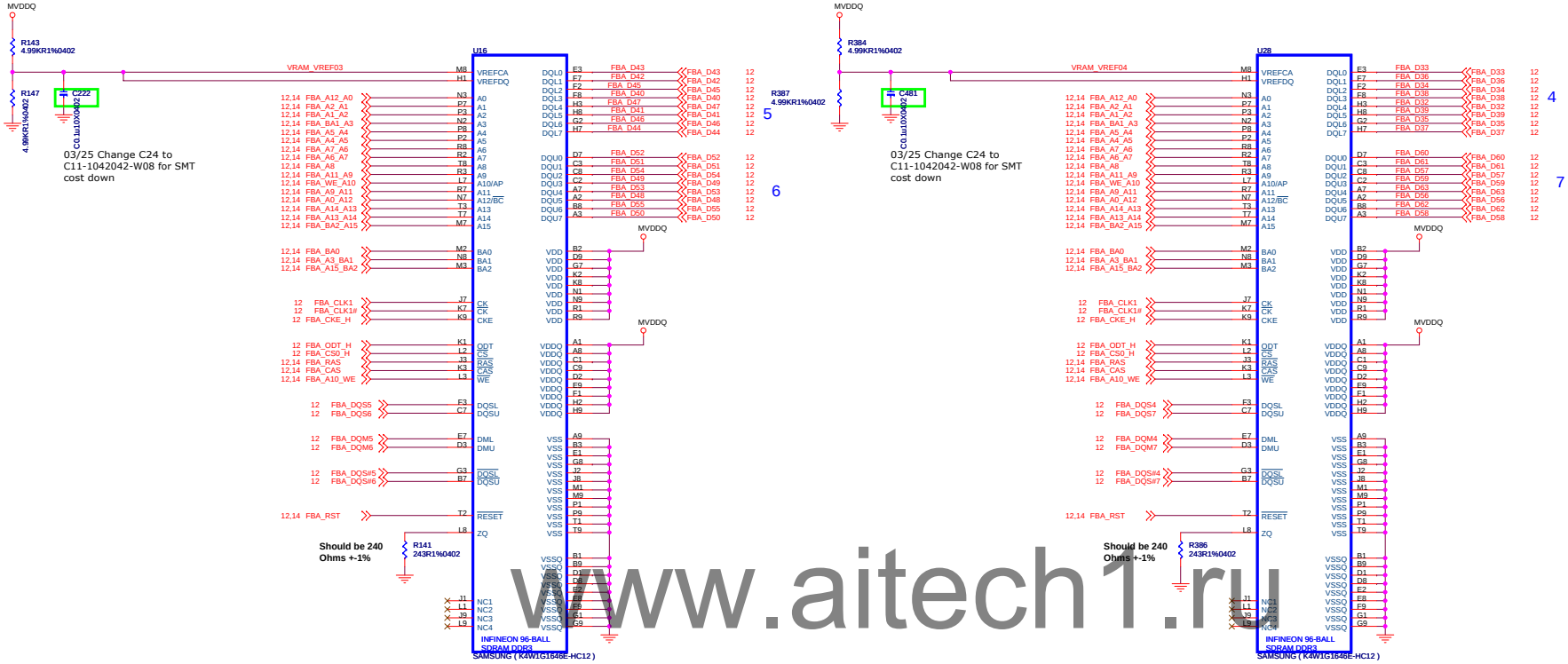
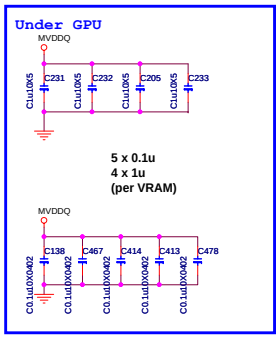
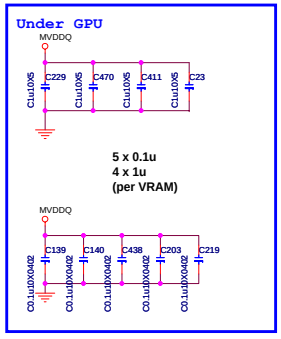




NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V

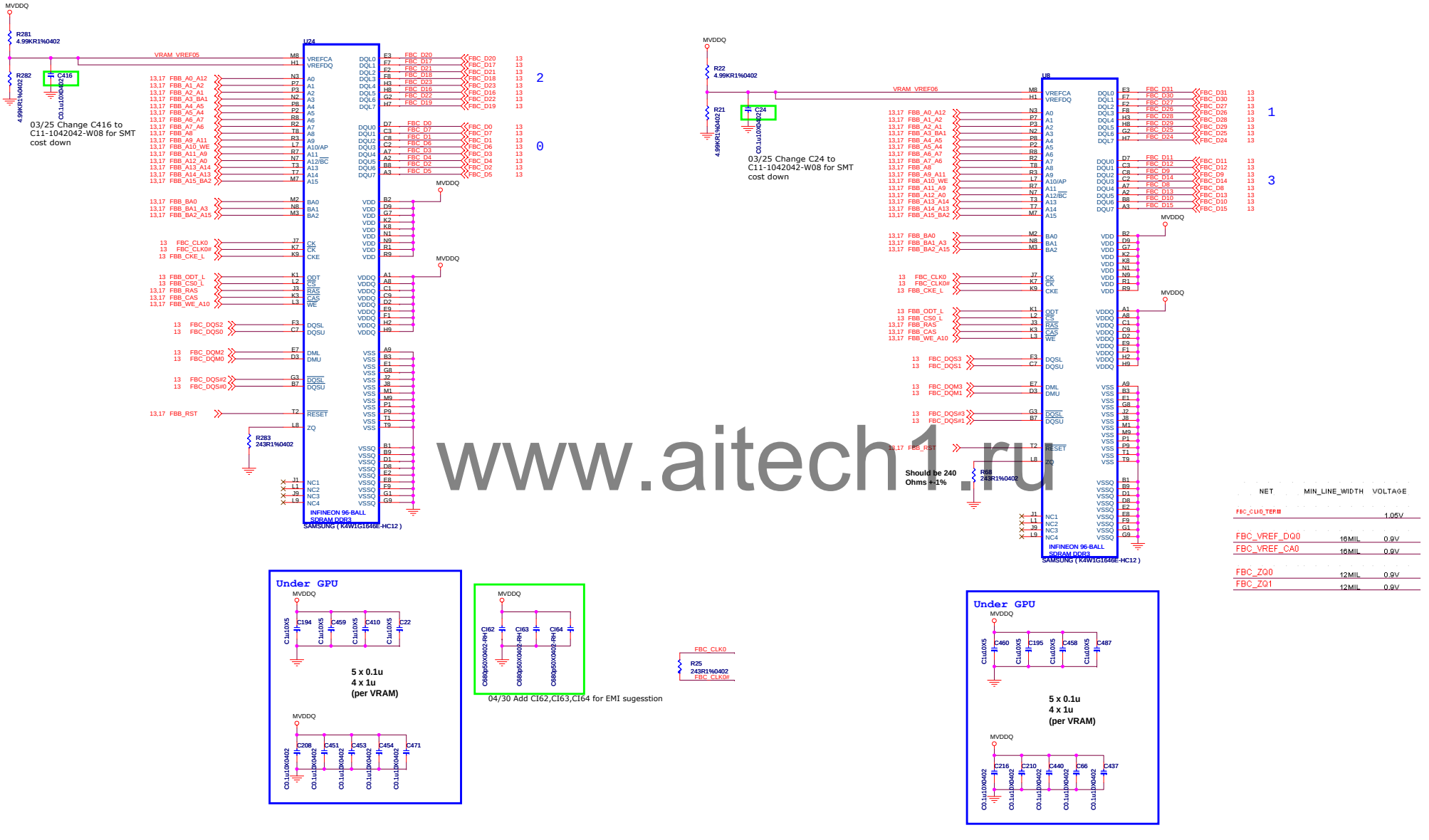


MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1 FrameA DDR3 II

Size: Custom | Document Number: MS-16G1 | Rev: 0.A

Date: Tuesday, May 04, 2010 | Sheet 15 of 56



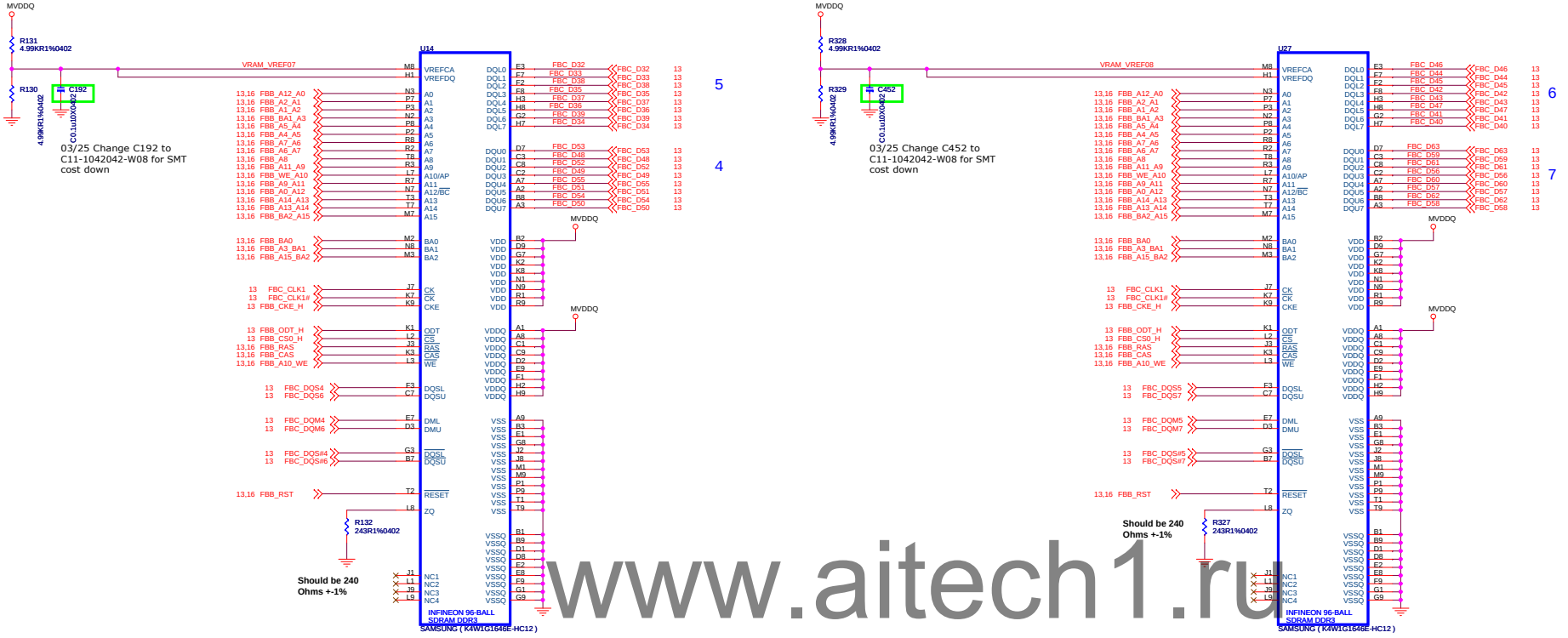
NET	MIN_LINE_WIDTH	VOLTAGE
FBC_CLK0_TERM		1.05V
FBC_VREF_DQ0	16MIL	0.9V
FBC_VREF_CA0	16MIL	0.9V
FBC_ZQ0	12MIL	0.9V
FBC_ZQ1	12MIL	0.9V

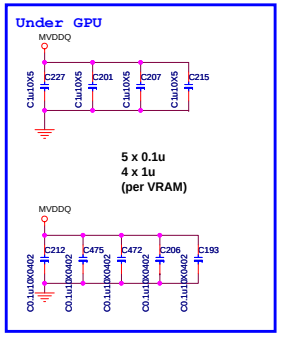
MICRO-STAR INT'L CO.,LTD.

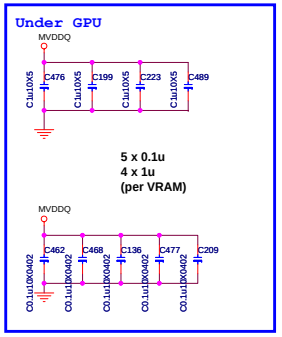
Title: N11P-GV1 FrameB DDR3 I

Size: Custom | Document Number: MS-16G1 | Rev: 1.0

Date: Tuesday, May 04, 2010 | Sheet 16 of 56





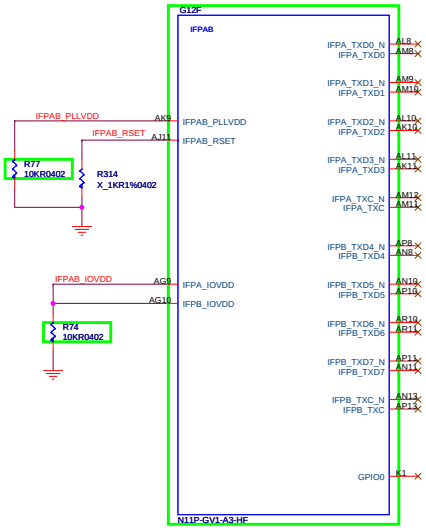


MICRO-STAR INT'L CO.,LTD.

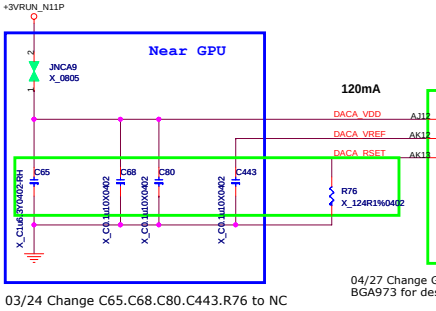
Title: N11P-GV1 FrameB DDR3 II

Size: Custom | Document Number: MS-16G1 | Rev: 1.0

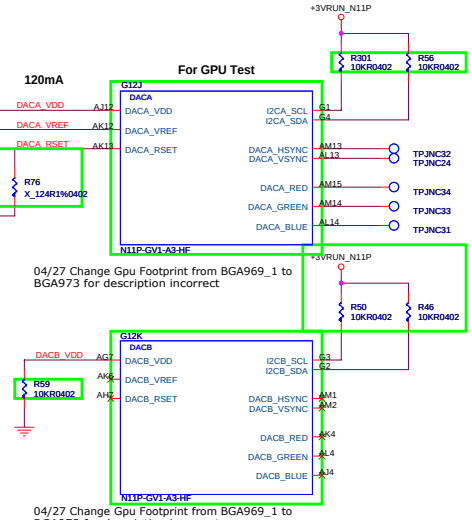
Date: Tuesday, May 04, 2010 | Sheet 17 of 56



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

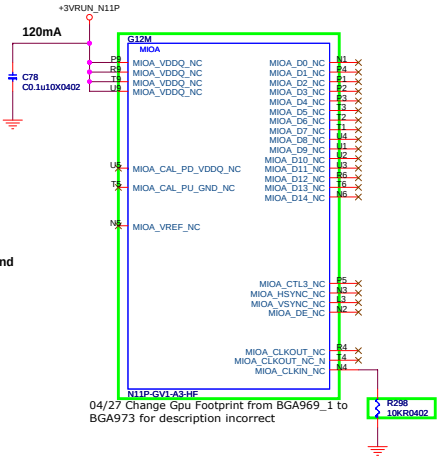


03/24 Change C65.C68.C80.C443.R76 to NC

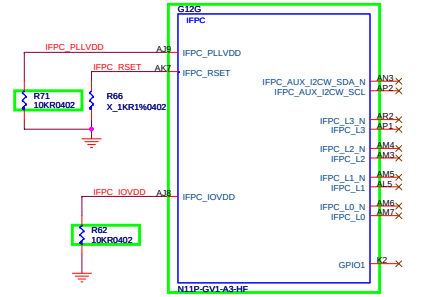


04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

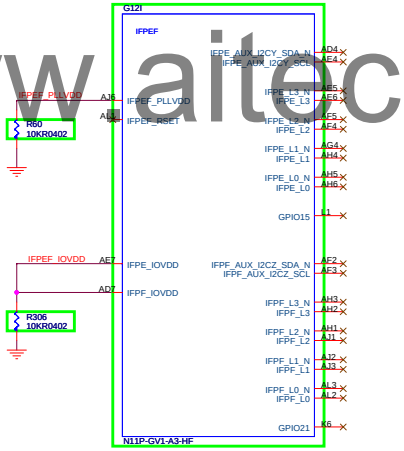
01/13 Nvidia Recommend



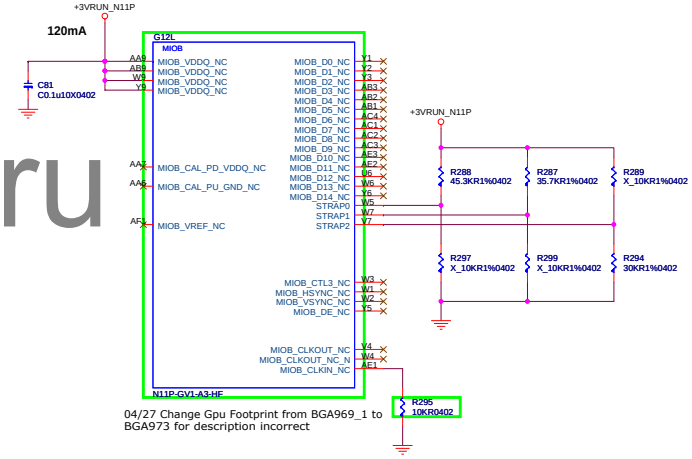
04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect



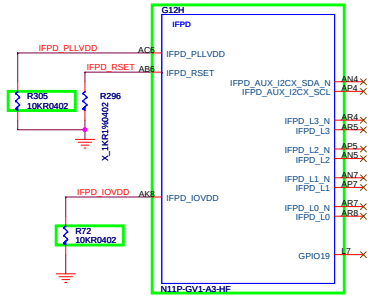
04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

Resistor Values	Pull-up to VDD	Pull-down to GND
5k Ω	1000	0000
10k Ω	1001	0001
15k Ω	1010	0010
20k Ω	1011	0011
25k Ω	1100	0100
30k Ω	1101	0101
35k Ω	1110	0110
45k Ω	1111	0111

Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1 Display Interface

Size: Custom | Document Number: MS-16G1 | Rev: 0A

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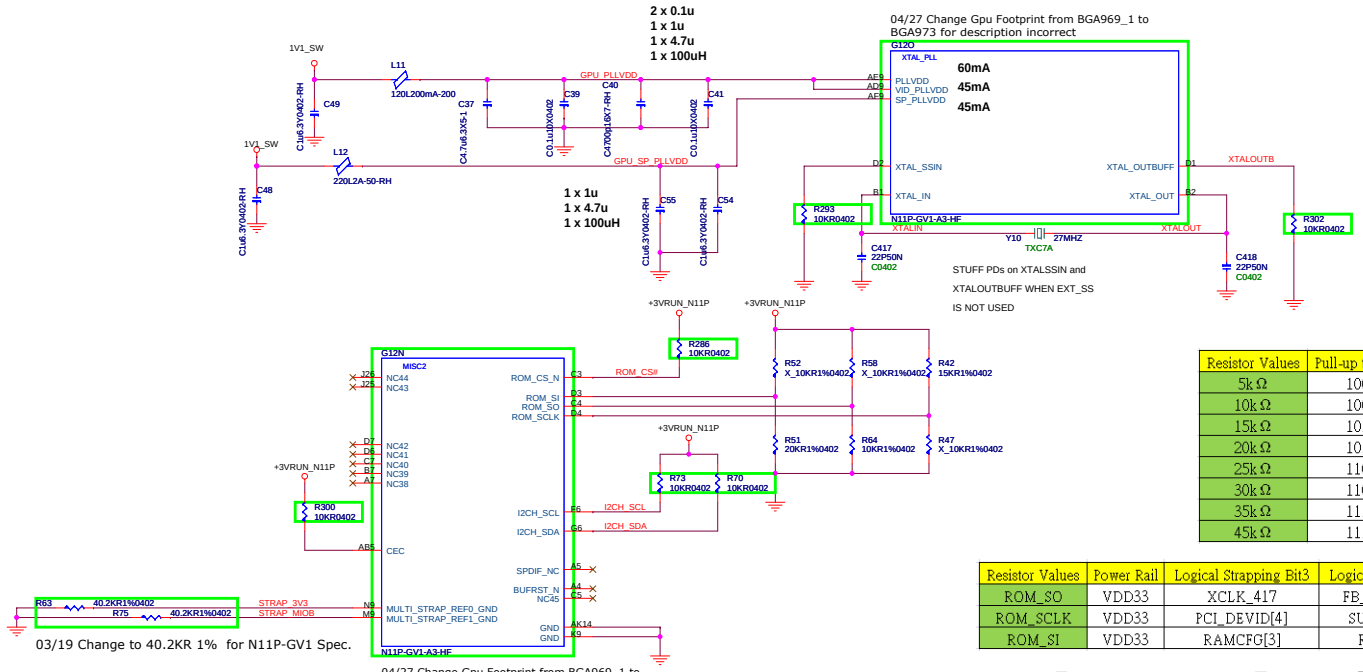


Resistor Values	Pull-up to VDD	Pull-down to GND
5k Ω	1000	0000
10k Ω	1001	0001
15k Ω	1010	0010
20k Ω	1011	0011
25k Ω	1100	0100
30k Ω	1101	0101
35k Ω	1110	0110
45k Ω	1111	0111

Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]

Ball Name	Availability	GB1-N11x Normal Function	I/O	Active	Function Description
GPIO0	GB1-64/128	General Purpose	N/A	N/A	
GPIO1	GB1-64/128	HPD-C	I		Hot plug detect for IFP link C
GPIO2	GB1-64/128	LCD0_BL_PWM	O	High	Panel backlight brightness(PWM capable)
GPIO3	GB1-64/128	LCD0_VDD	O	High	panel power enable
GPIO4	GB1-64/128	LCD0_BL_EN	O	High	Panel backlight On/Off(PWM capable)
GPIO5	GB1-64/128	GPU_VID0	O		GPU VID0
GPIO6	GB1-64/128	GPU_VID1	O		GPU VID1
GPIO7	GB1-64/128	GPU_VID2	O		GPU VID2
GPIO8	GB1-64/128	OVERT	I/O	Low	Thermal Catastrophic Overtemp
GPIO9	GB1-64/128	ALERT	I/O	Low	Thermal Alert
GPIO10	GB1-64/128	MEM_VREFF	O		Memory VREF switch
GPIO11	GB1-64/128	SLI_SYNC	I/O	Low	SLI raster sync
GPIO12	GB1-64/128	PWR_LEVEL	I		AC power detect input
GPIO13	GB1-64/128	MEM_VID	O		MEM_VID or Power supply control
GPIO14	GB1-64/128	PWR_CTRL1	O		Power supply control
GPIO15	GB1-64/128	HPD-E	I		Hot plug detect for IFP Link E
GPIO16	GB1-64/128	FAN_PWM	O		Programmable Fan Control
GPIO17	GB1-64/128	Reserved	I		
GPIO18	GB1-64/128	Reserved	I		
GPIO19	GB1-64/128	HPD-D	I		Hot plug detect for IFP Link D
GPIO20	GB1-64/128	Reserved	I		
GPIO21	GB1-64/128	HPD-F	I		Hot plug detect for IFP Link F
GPIO22	GB1-64/128	SWAPRDY	I		SLI swap ready signal
GPIO23	GB1-64/128	STEREO	I/O		

MICRO-STAR INT'L CO.,LTD.

Title: N11P-GV1 Thermal, GPIOs

Size: Custom | Document Number: MS-16G1 | Rev: 0A

Date: Tuesday, May 04, 2010 | Sheet 19 of 56

DA-04661-001_v04
DA-04882-001

Products	GPU (W)	Mem (W)	NVCLK/MCLK (MHz)
N11P-GE1 1024MB DDR3	22.98	5.07	575/790
N11P-LP1 1024MB DDR3	14.81	4.78	475/700
N11P-GS1 1024MB DDR3	22.85	4.97	450/790

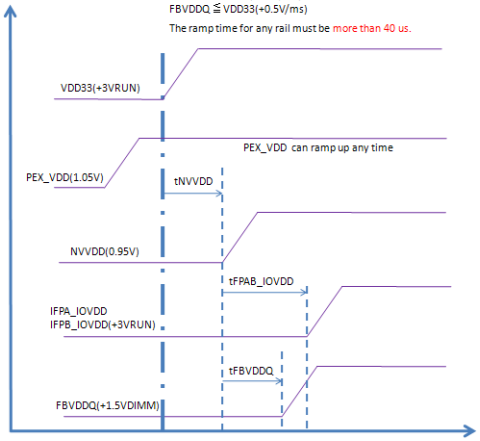
Products	NVVDD		
N11P-GE1 1024MB DDR3	0.95V	21.4A	20.33W
N11P-LP1 1024MB DDR3	0.85V	14.37A	12.22W
N11P-GS1 1024MB DDR3	0.9V	22.19A	19.97W

Products	FBVDD 1.5V		FBVDDQ GPU+Mem 1.5V	
N11P-GE1 1024MB DDR3	1.84A	2.76W	2.56A	3.84W
N11P-LP1 1024MB DDR3	1.69A	2.54W	2.48A	3.73W
N11P-GS1 1024MB DDR3	1.52A	2.28W	2.98A	4.48W

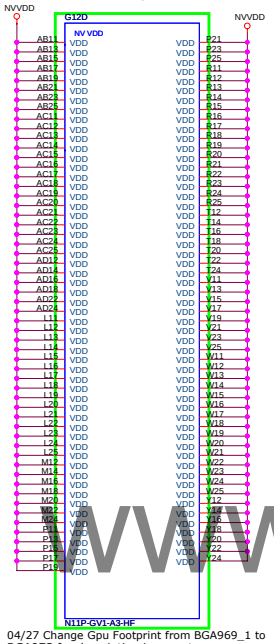
Products	PCI Express 1.05V		I/O PLLVDD 1.05V	
N11P-GE1 1024MB DDR3	599.27mA	0.63W	186.77mA	0.2W
N11P-LP1 1024MB DDR3	581.74mA	0.61W	186.77mA	0.2W
N11P-GS1 1024MB DDR3	578mA	0.61W	186mA	0.2W

Products	I/O PLLVDD 1.8V	
N11P-GE1 1024MB DDR3	88.5mA	0.16W
N11P-LP1 1024MB DDR3	88.5mA	0.16W
N11P-GS1 1024MB DDR3	87mA	0.16W

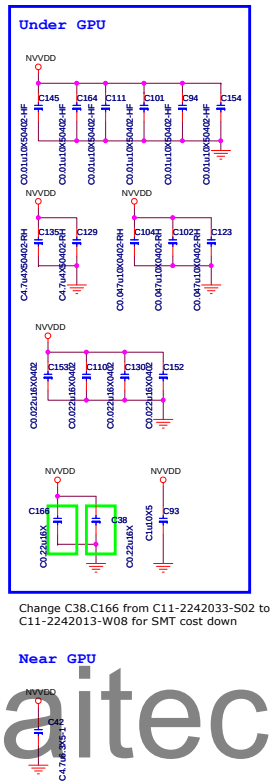
Products	Other 3.3V	
N11P-GE1 1024MB DDR3	39.97mA	0.13W
N11P-LP1 1024MB DDR3	39.97mA	0.13W
N11P-GS1 1024MB DDR3	39mA	0.13W



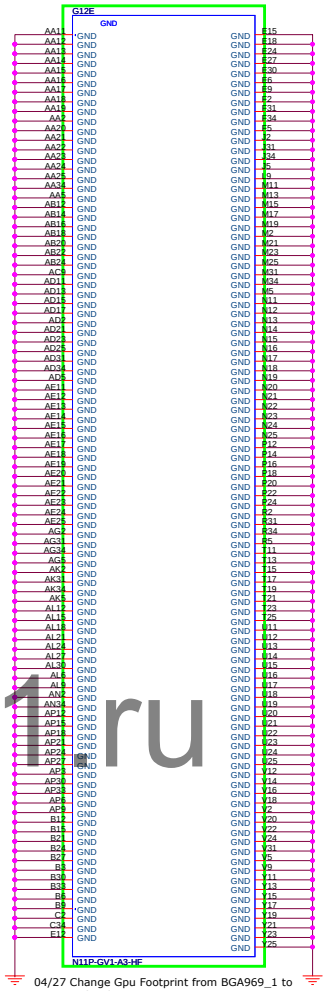
2 x 4700p
6 x 0.01u
4 x 0.022u
3 x 0.047u
2 x 0.22u
1 x 1u
1 x 4.7u



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect



Change C38.C166 from C11-2242033-S02 to C11-2242013-W08 for SMT cost down



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05 V) (6) (mA)	PCI Express (1.05 V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3 V) (mA)	Other (3.3 V) (W)
N11P-GV1 (128-bit, 1024 MB, DDR3)	16.01	4.72	450/700	0.85	15.82	13.45	1.66	2.49	2.47	3.71	572	0.60	88.50	0.16	186.77	0.20	39.97	0.13

MICRO-STAR INT'L CO.,LTD.
Title: N11P-GV1 Power & GND
Size: Custom | Document Number: MS-16G1 | Rev: 0A
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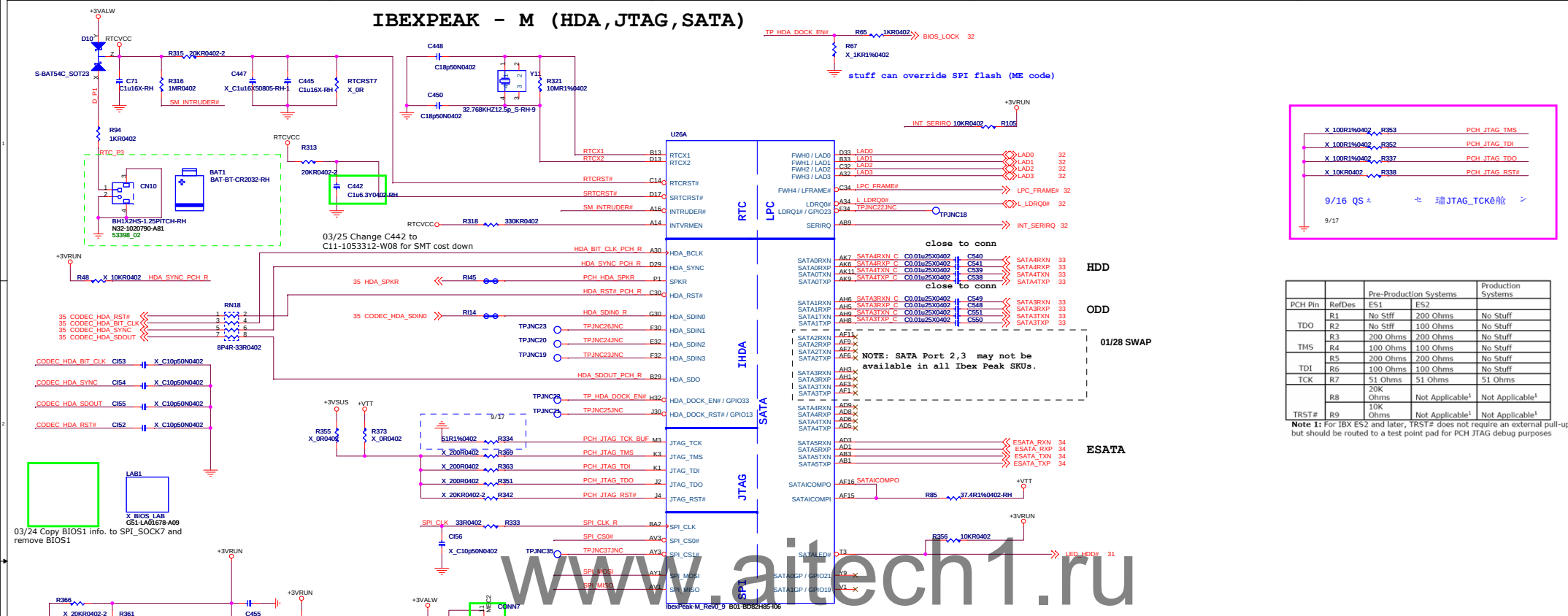
IBEXPEAK - M (HDA,JTAG,SATA)



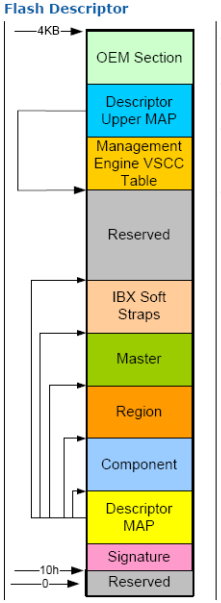
Boot Flow for Ibex Peak

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x0. The descriptor fetch is triggered whichever comes first, the assertion of MEPWROK or deassertion of LAN_RST#. If the signature is present and valid, then the PCH controller will boot in Descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the GNT0# and SPI_CS1#1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from Firmware hub or SPI flash.

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Ibex Peak based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.

Flash Descriptor



- The Flash signature at the bottom of the flash (offset 0) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. This table is NOT used by Intel® ME Ignition FW only. BIOS and GbE write and erase capabilities depend on LVSCC and UVSCC registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

		Pre-Production Systems	Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

Region Access Control Table

Master Read/Write Access			
Region	CPU and BIOS	ME	GbE Controller
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Management Engine	Read / Write	ME can always read from and write to ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (HDA,JTAG,SATA)

Size: Custom | Document Number: MS-16G1 | Rev: 0A

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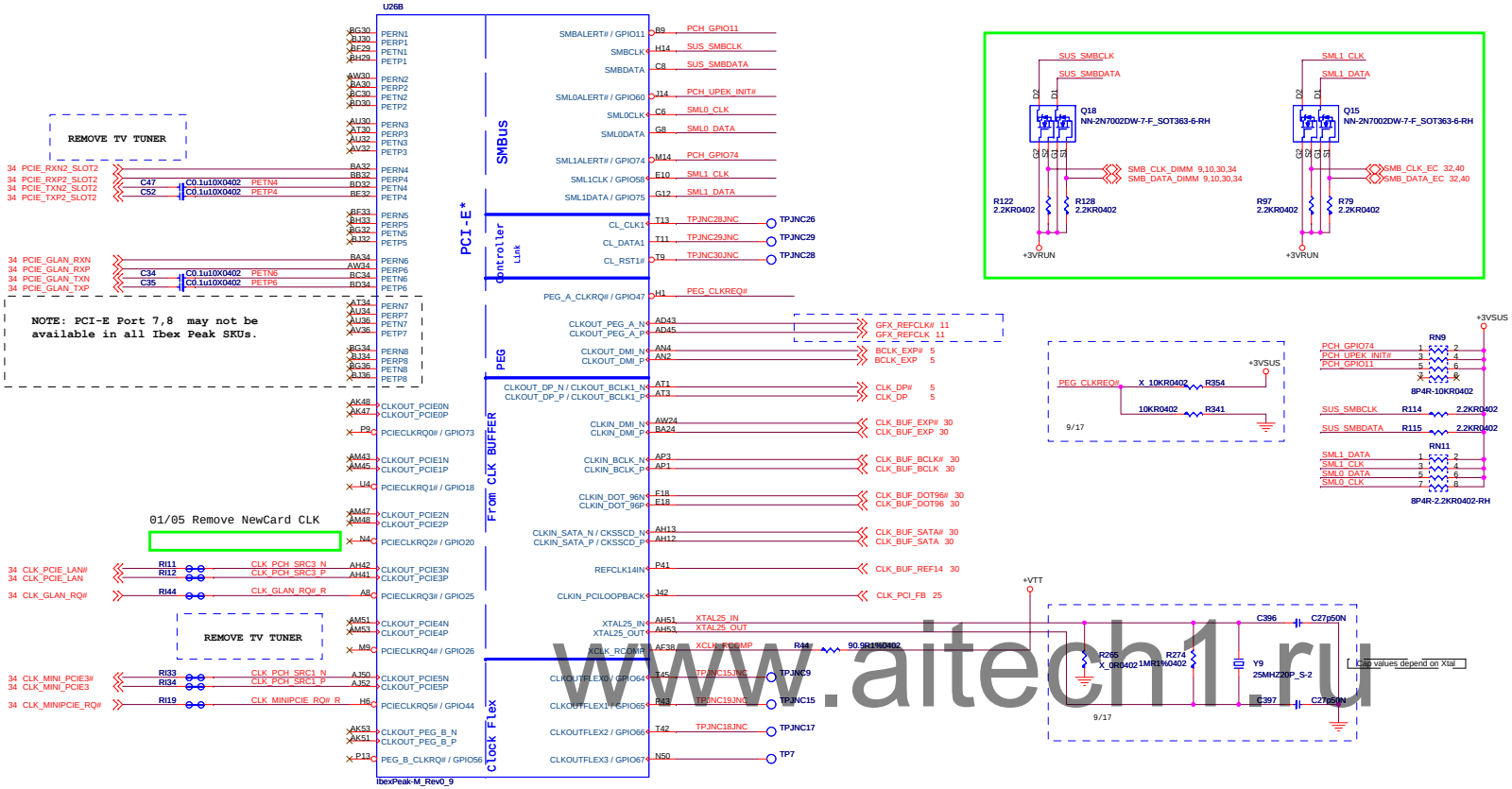
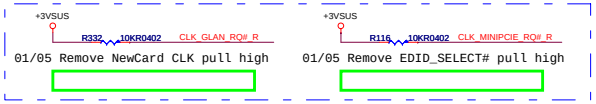
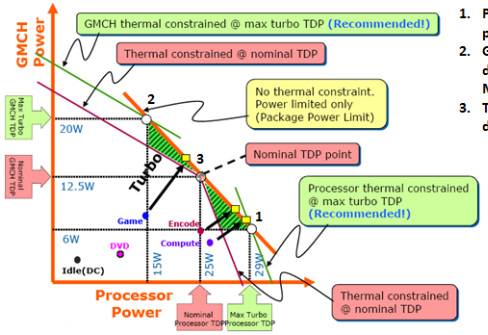
IBEXPEAK - M (PCI-E,SMBUS,CLK)



PCIECLKRQ1# / GPIO18 PCIECLKRQ2# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

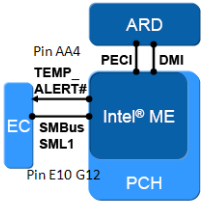
01/28 Add CLK_MINIPCIE_RQ# Pull-High





- The system can be maximized turbo benefit by: Thermal design for package turbo limits
- Caution: Designs managing only the nominal TDP point will be under-designed for package turbo!
- Cooling component TDPs ≠Enabling Package Turbo

1. Processor turbo – Most challenging in terms of power density, drives Heat Exchanger design
2. GFX turbo – Doesn't affect Heat Exchanger design, just ensures that Thermal Interface Material is capable
3. TDP (Legacy) – Slightly relaxed Heat Exchanger design



- Turbo Boost control– EC passes parameters through PCH to host software for real-time Turbo Boost control.
- PCH can be programmed to notify EC when a device is outside of limits via TEMP_ALERT# signal– No SW alert in PCH.

- EC can read from PCH via SMBus:
  - Temperatures
    - CPU, GMCH
  - Sequence number
  - Host status
- EC can write to PCH via SMBus:
  - Disable and enable power sharing
  - CPU and package power clamps
  - Biasing preference
  - Upper and lower temperature limits
    - CPU, MCH
    - TEMP_ALERT# trip points
- PCH can alert EC to out of range temperature conditions
  - TEMP_ALERT# signal assertion
- EC can monitor Intel® ME health by checking "Sequence Number"
  - Increments each time the Intel ME refreshes data

Indicates optional usage with Turbo Boost

Block Read Data Structure

Byte	Data	Format	Units	Range
0	Max Package Temperature	Unsigned byte	1°C/bit	0-255°C
1	PCH Temperature	Unsigned byte	1°C/bit	0-255°C
3:2	CPU Temperature	10.6 Format	1/64°C/bit	0-256°C
4	MCH Temperature	Unsigned byte	1°C/bit	0-255°C
5	DIMM0 Temperature	Unsigned byte	1°C/bit	0-255°C
6	DIMM1 Temperature	Unsigned byte	1°C/bit	0-255°C
7	DIMM2 Temperature	Unsigned byte	1°C/bit	0-255°C
8	DIMM3 Temperature	Unsigned byte	1°C/bit	0-255°C
9	Sequence Number	Unsigned byte	Count	0-255
13:10	CPU Energy Counter	16 int:16frac	0.1253J/bit	
19:14	Host Status	Status register	N/A	N/A

EC-PCH Write Commands

Commands	Format	Units
SMBus Turbo Status (STS)	Register	
CPU Temperature Limits	10.6 Format	1/64°C/bit
MCH Temperature Limits	Unsigned byte	1°C/bit
IBX Temperature Limits	Unsigned byte	1°C/bit
DIMM Temperature Limits	Unsigned byte	1°C/bit
Processor Power Clamp	Unsigned word	0.1W/bit

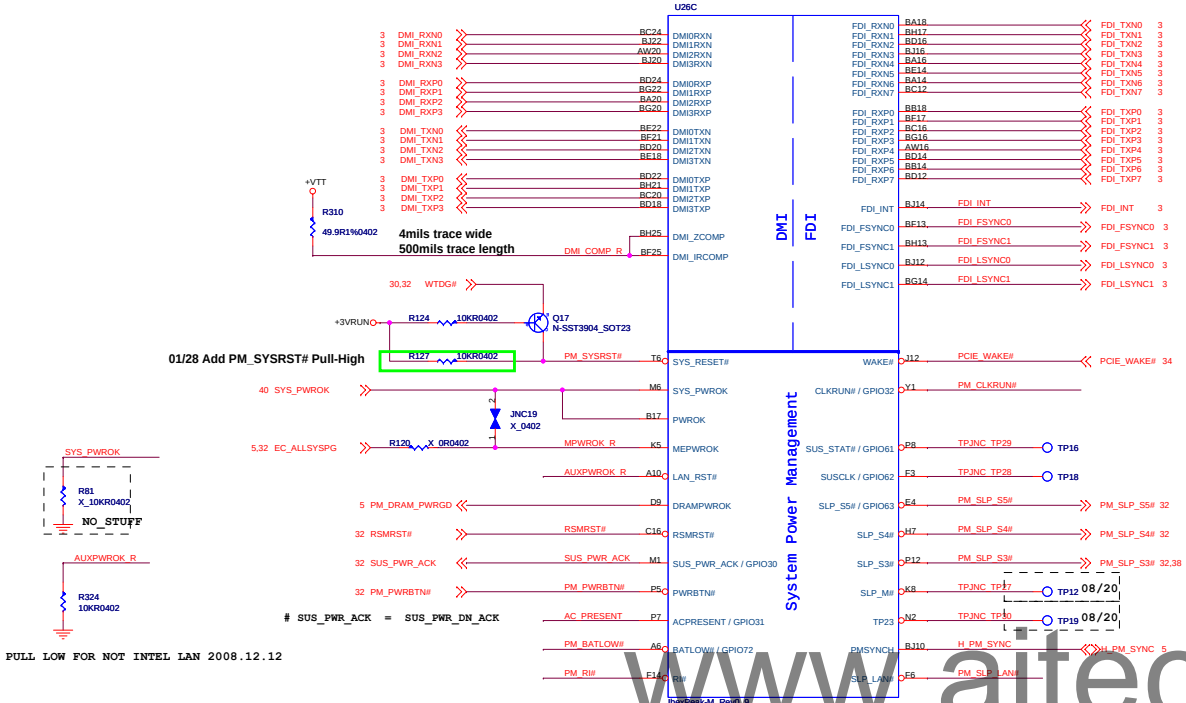
MICRO-STAR INT'L CO.,LTD.

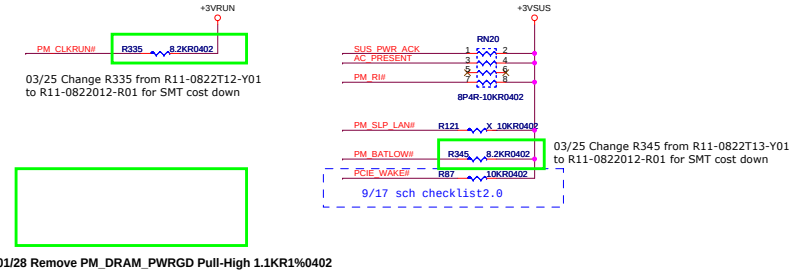
Title: IBEXPEAK - M (PCI-E,SMBUS,CLK)

Size: Custom | Document Number: MS-16G1 | Rev: 0A

Date: Tuesday, May 04, 2010 | Sheet 22 of 56

IBEXPEAK - M (DMI,FDI,GPIO)

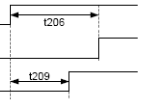




Flexible Display Interface

The Flexible Display Interface (Intel® FDI) is a bus technology that utilizes differential signaling to transport display data from a pixel source Havendale to a sink Ibex Peak. There are two Flexible Display Interface channels- A and B which are independently controlled. Each channel from Havendale include 4 Tx differential pairs comprising the data link, used for transporting pixel and framing data from the display engine. Two single-ended LineSync and FrameSync inputs. Single-ended DISP_INT is used for interrupts from sink (Ibex Peak) to source (Havendale).

Source	Dest	Signal Name
Board	PCH	PWROK
PCH	Processor	DRAMPWRGD
PCH	Processor	PROCPWRGD



Sym	Parameter	Min	Max	Units	Notes
t209	PWROK active to PROCPWRGD active	See Note 7	—	ms	7
t206	PWROK deglitch time	1	—	ms	6

6. Ensure PWROK is a solid logic '1' before proceeding with the boot sequence. Note: If PWROK drops after t206 it will be considered a power failure.
7. t209 minimum timing selectable as 1 ms (recommended), 5 ms, 50 ms, or 100 ms using bits 9:8 of PCHSTRP15.

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (DMI,FDI,GPIO)

Size: Custom | Document Number: MS-16G1 | Rev: 0A

Date: Tuesday, May 04, 2010 | Sheet 23 of 56

IBEXPEAK - M (LVDS,DDI)

DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

02/08 Remove pull high resister LVDS Connector side already have.

LVDS_BLON
R20 X_100KR0402
10/27 0B

03/26 Change R41 and R39 Footprint from 0R0402 to NC_0402_6 for cost down

Place near PCH
R45 2.37KR1%0402-RH

1.MXM only LVD_IBG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCTX_LVD can be connected to GND.

2.If use LVDS, LVD_IBG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCTX_LVD connect to power.

LVDS_VDD_EN
R32 X_100KR0402

CRT_B_UMA
CRT_G_UMA
CRT_R_UMA
CI9 C10p50N0402
CI13 C10p50N0402
CI12 C10p50N0402
12/24 EMI suggestion

04/30 Change CI12,CI13,CI9 to stuff for EMI suggestion

CRT_B_UMA
CRT_G_UMA
CRT_R_UMA
R273 150R1%0402
R272 150R1%0402
R271 150R1%0402
CLOSE TO CHIP PCH

+3VRUN
R270 X_2.2KR0402 CRT_CLK_UMA
R264 X_2.2KR0402 CRT_DATA_UMA

37.5ohm : 7/10/20 , 8/10/20 , 800mils

U26D

LVDS:
31 LVDS_BLON
31 LVDS_VDD_EN
L_BKLTEN
L_VDD_EN
L_BKLTCTL
31 LVDS_DDC_CLK
31 LVDS_DDC_DATA
LVDS_DDC_CLK
LVDS_DDC_DATA
L_DDC_CLK
L_DDC_DATA
TPJNC14
TPJNC13
TPJNC16JNC
TPJNC14JNC
L_CTRL_CLK
L_CTRL_DATA
TPJNC16
TP_LVDS_IBG
TPJNC21JNC
LVD_IBG
LVD_VBG
R41
R39
LVD_VREFH
LVD_VREFL
31 LVDSA_CLK#
31 LVDSA_CLK
LVDSA_CLK#
LVDSA_CLK
31 LVDSA_DATA0#
31 LVDSA_DATA1#
31 LVDSA_DATA2#
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
31 LVDSA_DATA0
31 LVDSA_DATA1
31 LVDSA_DATA2
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3
31 LVDSB_CLK#
31 LVDSB_CLK
LVDSB_CLK#
LVDSB_CLK
31 LVDSB_DATA0#
31 LVDSB_DATA1#
31 LVDSB_DATA2#
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
31 LVDSB_DATA0
31 LVDSB_DATA1
31 LVDSB_DATA2
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT:
34 CRT_B_UMA
34 CRT_G_UMA
34 CRT_R_UMA
CRT_BLUE
CRT_GREEN
CRT_RED
34 CRT_CLK_UMA
34 CRT_DATA_UMA
CRT_DDC_CLK
CRT_DDC_DATA
34 CRT_HSYNC_UMA
34 CRT_VSYNC_UMA
RI35
RI32
HSYNC
VSYNC
CRT_HSYNC
CRT_VSYNC
DAC_IREF_R
R24 1KR1%0402
DAC_IREF
CRT_IRTN

LO note: Place near PCH

ibexPeak-M_Rev0_9

Digital Display Interface:
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA
SDVO_CTRL_CLK
SDVO_CTRL_DATA
R268 X_20KR1%0402
R269 X_20KR1%0402
+3VRUN
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P
DDPD_CTRLCLK
DDPD_CTRLDATA
HDMI_SCL 34
HDMI_SDA 34
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
TPJNC13JNC
TPJNC11JNC
TPJNC11
TPJNC12
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P
DPD_LANE2_N_C
DPD_LANE2_P_C
DPD_LANE1_N_C
DPD_LANE1_P_C
DPD_LANE0_N_C
DPD_LANE0_P_C
DPD_LANEC_N_C
DPD_LANEC_P_C
C420 C0.1u10X0402
C419 C0.1u10X0402
C422 C0.1u10X0402
C421 C0.1u10X0402
C424 C0.1u10X0402
C427 C0.1u10X0402
C423 C0.1u10X0402
C426 C0.1u10X0402
DPD_LANE2_N 34
DPD_LANE2_P 34
DPD_LANE1_N 34
DPD_LANE1_P 34
DPD_LANE0_N 34
DPD_LANE0_P 34
DPD_LANEC_N 34
DPD_LANEC_P 34

+3VRUN
HDMI_SDA R12 4.7KR0402
HDMI_SCL R13 4.7KR0402
DVI_A_HPD_R RI13
HDMI_HPD 34
R43 110KR1%0402-RH

MICRO-STAR INT'L CO.,LTD.
Title: IBEXPEAK - M (LVDS,DDI)
Size: Custom
Document Number: MS-16G1
Rev: 0A
Date: Tuesday, May 04, 2010
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IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCI_GNT#0
PCI_GNT#1
R34 X_1KR0402
R23 X_1KR0402
PCI_GNT#3
R17 X_1KR0402
DGPU_PWM_SELECT#
R53 X_1KR0402

U26E

PCI
NVRAM
USB

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
C/BE0# C/BE1# C/BE2# C/BE3#
PIRQA# PIRQB# PIRQC# PIRQD#
REQ0# REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54
GNT0# GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55
PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5
PCIRST#
SERR# PERR#
IRDY# PAR DEVSEL# FRAME#
PLOCK#
STOP# TRDY#
PME#
PLTRST#
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0 / NV_IO0 NV_DQ1 / NV_IO1 NV_DQ2 / NV_IO2 NV_DQ3 / NV_IO3 NV_DQ4 / NV_IO4 NV_DQ5 / NV_IO5 NV_DQ6 / NV_IO6 NV_DQ7 / NV_IO7 NV_DQ8 / NV_IO8 NV_DQ9 / NV_IO9 NV_DQ10 / NV_IO10 NV_DQ11 / NV_IO11 NV_DQ12 / NV_IO12 NV_DQ13 / NV_IO13 NV_DQ14 / NV_IO14 NV_DQ15 / NV_IO15
NV_ALE NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE# NV_WR#1_RE#
NV_WE#_CK0 NV_WE#_CK1

NV_RCOMP
R346 X_32.4R1%0402-RH

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
USBRBIAS# USBRBIAS
USB_BIAS
R311 22.6R1%0402
+3VSUS

USB_P0N 34 USB_P0P 34 USB_P1N 34 USB_P1P 34 — 00_USB 01_eSATA_USB
USB_P3N 34 USB_P3P 34 USB_P4N 31 USB_P4P 31 USB_P5N 34 USB_P5P 34 — 03_USB 05_WiFi
USB_P10N 34 USB_P10P 34 USB_P11N 34 USB_P11P 34 USB_P12N 33 USB_P12P 33 — 11_BT

NOTE: USB Port 6,7 may not be available in all Ibex Peak SKUs.

EHCI 1 : 0~7
EHCI 2 : 8~13

OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14
USB_OC#
R88 10KR0402

IbexPeak-M_Rev0_9

INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD#
PCI_REQ#0 PCI_REQ#1 PCI_REQ#2 PCI_REQ#3
PCI_GNT#0 PCI_GNT#1 PCI_GNT#3
DGPU_PWM_SELECT#
INT_PIRQE# INT_PIRQF# INT_PIRQG# INT_PIRQH#
PCI_SERR# PCI_PERR#
PCI_IRDY#
PCI_DEVSEL# PCI_FRAME#
PCI_LOCK#
PCI_STOP# PCI_TRDY#
TP17 TPJNC_TP26
PLT_RST#

CLK_PCIF_PORT80
CLK_PCI_KBC
CLK_PCI_FB
CI47 X_C0.1u16Y0402
CI16 X_C0.1u16Y0402
CI48 X_C0.1u16Y0402
12/24
EMI suggestion

22 CLK_PCI_FB
32 CLK_PCI_KBC
32 CLK_PCIF_PORT80
CLK_PCI_FB R262 22R0402 CLKOUT_PCI1
CLK_PCI_KBC R35 22R0402 CLKOUT_PCI2
CLK_PCIF_PORT80 R261 22R0402 CLKOUT_PCI3

+3VRUN
RN15 PCI_REQ#1 PCI_FRAME# PCI_TRDY# INT_PIRQH# — 8P4R-8.2KR0402-1
RN14 PCI_REQ#0 INT_PIRQB# INT_PIRQF# PCI_REQ#3 — 8P4R-8.2KR0402-1
RN17 INT_PIRQG# INT_PIRQC# INT_PIRQE# PCI_STOP# — 8P4R-8.2KR0402-1
RN7 PCI_LOCK# PCI_PERR# PCI_DEVSEL# INT_PIRQA# — 8P4R-8.2KR0402-1
RN16 PCI_IRDY# PCI_SERR# INT_PIRQD# PCI_REQ#2 — 8P4R-8.2KR0402-1
DGPU_PWM_SELECT# R49 10KR0402

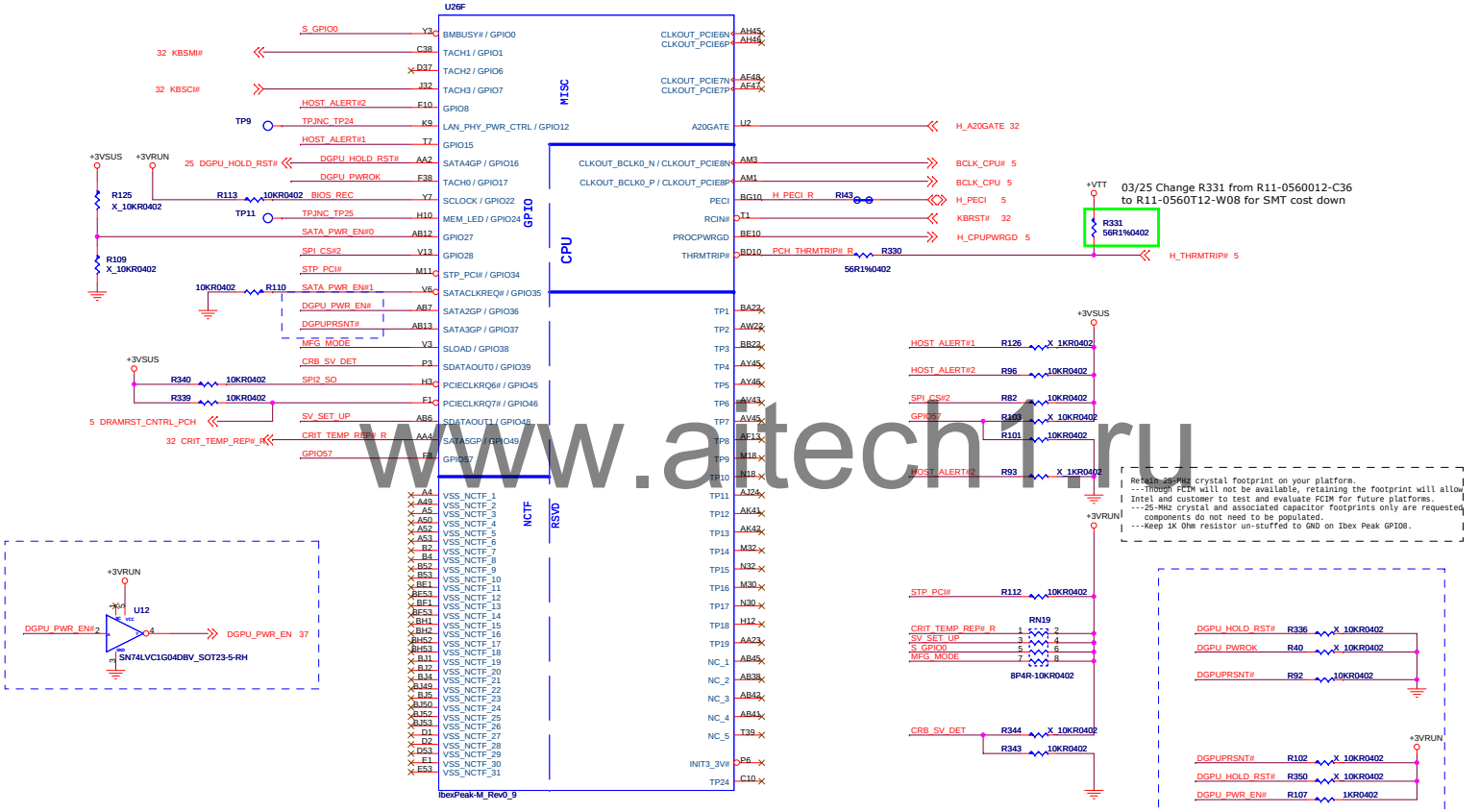
+3VSUS
C160 C0.1u10X0402
U11 S08P5X_SC70
PLT_RST#
26 DGPU_HOLD_RST#
32 DGPU_HOLD_RST#_EC
R362 X_0R0402
PCIE_RST# 11

+3VSUS
C165 C0.1u10X0402
U13 S08P5X_SC70
RN12 8P4R-33R0402
WLAN_RST# 34
LPC_RST# 32
LAN_RST# 34
RI24
BUF_PTL_RST# 5

MICRO-STAR INT'L CO.,LTD.

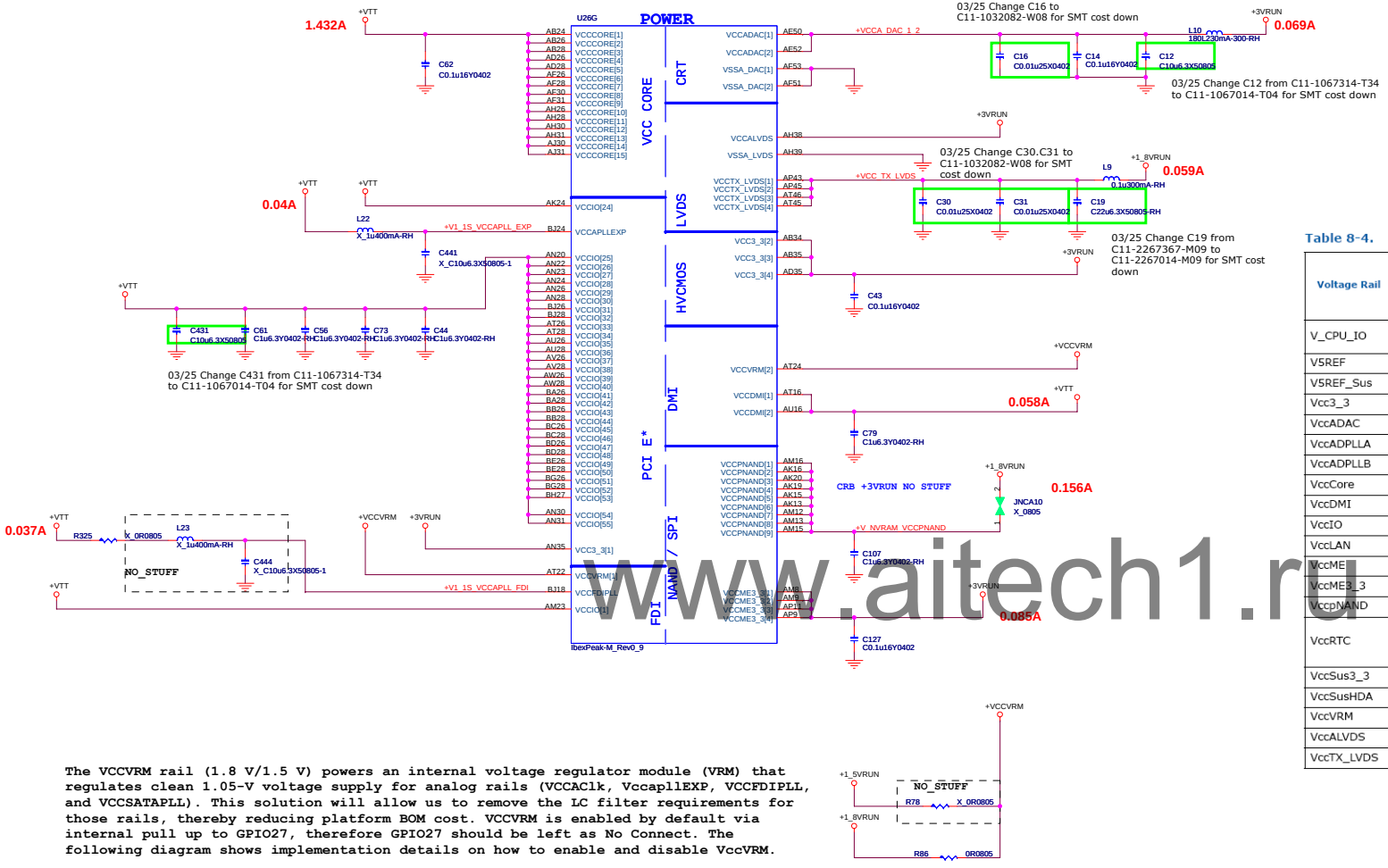
Title	IBEXPEAK - M (PCI,USB,NVRAM)	
Size: Custom	Document Number: MS-16G1	Rev: 0A
Date: Tuesday, May 04, 2010	Sheet 25 of 56	

IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)		
Size: Custom	Document Number: MS-16G1		Rev: 0A
Date: Tuesday, May 04, 2010	Sheet 26 of 56		

IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCACLk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

Mobile Thermal Design Power

SKU	Thermal Design Power (TDP)	Notes
QM57	3.5 W	1
HM57	3.5 W	1
HM55	3.5 W	1
PM55	3.5 W	1
QS57	3.4 W	1

Table 8-4. Measured I_{CC} (Mobile Only)

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
V_CPU_IO	1.1/ 1.05	.001	.001	.001	.001			—
V5REF	5	.001	.001	.001	.001			—
V5REF_Sus	5	.001	.001	.001	.001	.001		—
Vcc3_3	3.3	.305	.305	.0176	.0176			—
VccADAC	3.3	.075	.0011	.0011	.0011			—
VccADPLLA	1.05	.088	.0176	.825	.0044			—
VccADPLLB	1.05	.088	.0176	.0044	.0044			—
VccCore	1.05	1.43	1.254	.3685	.2805			—
VccDMI	1.1	.055	.055	.0011	.0011			—
VccIO	1.05	3.23	2.628	.463	.285			—
VccLAN	1.05	.220	.220	.066	.066	.132		—
VccME	1.05	1.2	1.2	.186	.186	.98	.0044	—
VccME3_3	3.3	.031	.031	.0022	.0022	.0154	.0022	—
VccpNAND	1.8	.0055	.0055	.0022	.0022			—
VccRTC	3.3	.0011	.0011	.0011	.0011	.0011	.0011	6 uA See notes 1, 2
VccSus3_3	3.3	.087	.087	.0132	.0132	.133	.0297	—
VccSusHDA	3.3	.0088	.0088	.001	.001	.001	.001	—
VccVRM	1.8/1.5	.156	.114	.113	.045			—
VccALVDS	3.3	.0011	.0011	.0011	.0011			
VccTX_LVDS	1.8	.066	.0011	.0198	.0011			

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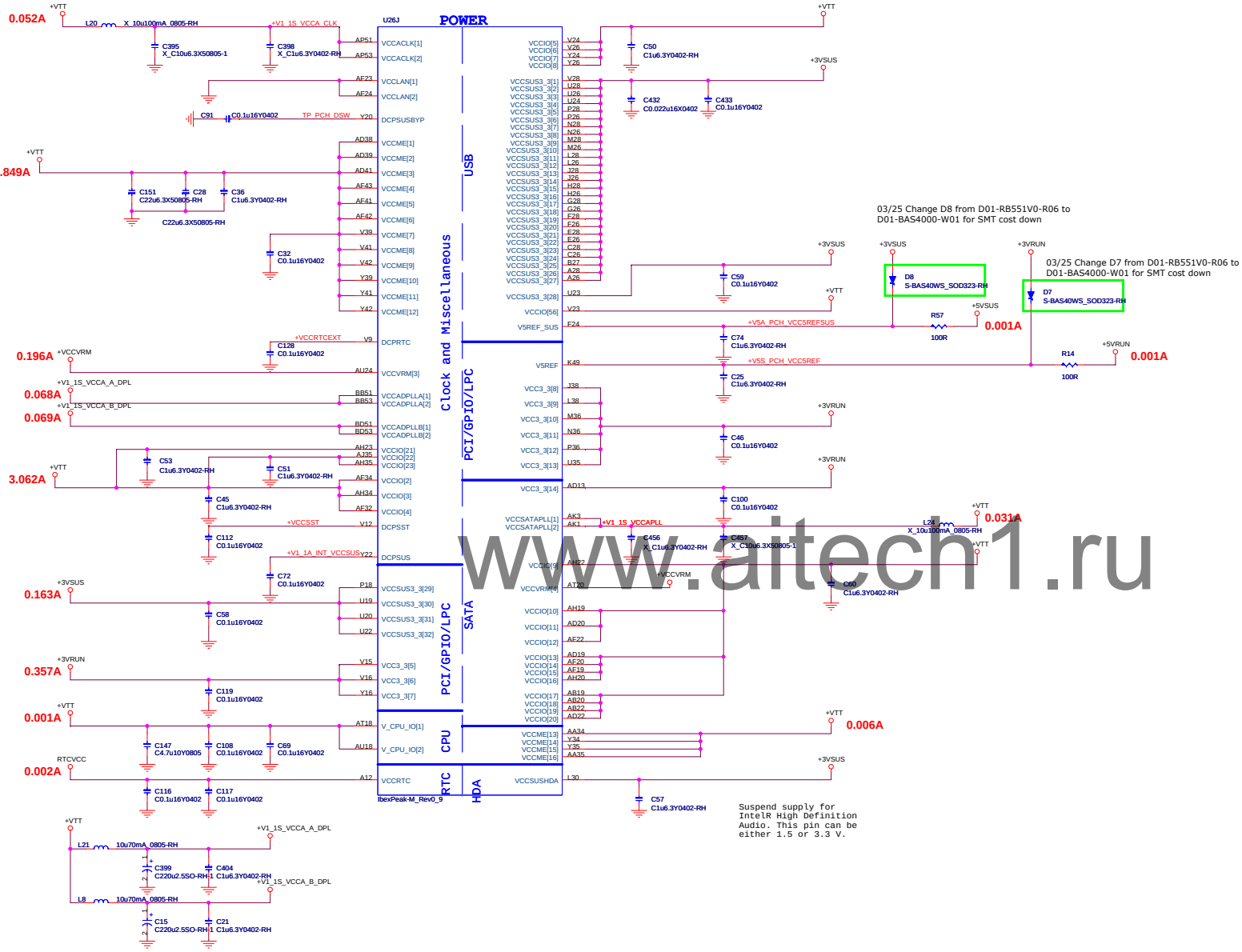
VccLAN may be grounded if Intel LAN is disabled.

IBEXPEAK - M (POWER)



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (POWER)		
Size: Custom	Document Number: MS-16G1		Rev: 0A
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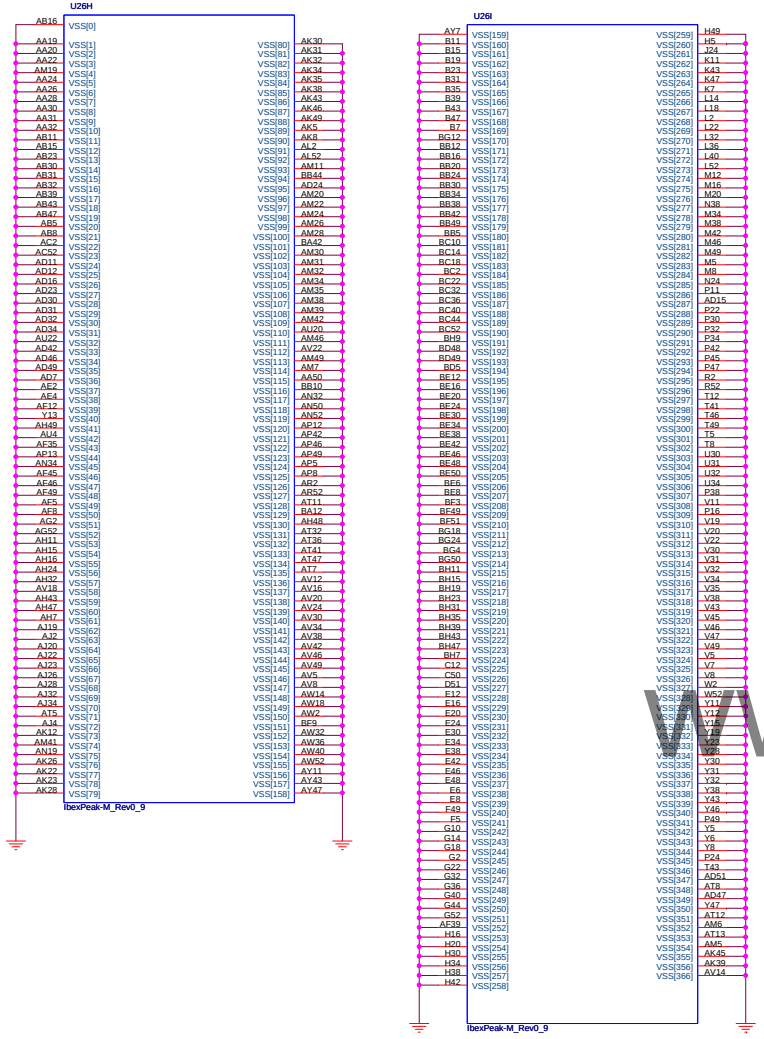
IBEXPEAK - M (GND)



Intel® 5 Series Chipset Mobile SKUs

Feature Set		SKU Name(s)				
		QM57	HM57	PM55	HM55	QS57
PCI Express* 2.0 Ports		8	8	8	6[5]	8
USB* 2.0 Ports		14	14	14	12[4]	14
SATA Ports		6	6	6	4[6]	6
HDMI/DVI/VGA/SDVO/DisplayPort		Yes	Yes	No	Yes	Yes
LVDS		Yes	Yes	No	Yes	Yes
Graphics Support with PAVP 1.5		Yes	Yes	No	Yes	Yes
FIS Based Port Multiplier Support		Yes	Yes	Yes	No	Yes
Intel® Quiet System Technology		No	No	No	No	No
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	Raid 0/1/5/10 Support	Yes	Yes	Yes	No	Yes
Intel® ME Ignition FW only		No	No	Yes	No	No
Intel® AT		Yes	Yes	No	Yes	Yes
Intel® AMT 6.0		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Business		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Consumer		No	Yes	No	No	No
Intel® Remote Wake Technology		No	No	No	No	No

Figure 2-6. Platform Power Block Diagram—S3, M-Off, with WoL, No WoWLAN

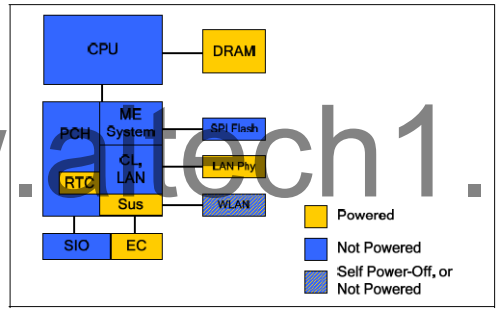


Figure 2-9. Platform Power Block Diagram—S4-5, M-Off, with WoL, No WoWLAN

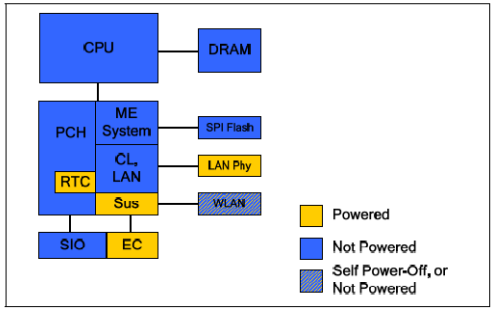


Table 113. Power Delivery Summary for Intel Management Engine SubSystem (Sheet 1 of 2)

What It Powers	Rail	Sx[1]/M3	Sx/Moff[2]	Sx/Moff/WOL[3]	Source	Enabled By	Power OK indicator
Platform 5-V Rail	V5.0A	On	On	On	5 V Always (Sx)		
DRAM VDD	V1.5U	On in S3	On in S3	On in S3	V1.5U	SLP_S4#	
DRAM VTT	V0.75S or V0.75U	Off[4]	Off[4]	Off[4]	V0.75S or V0.75U	SLP_S3#	
CK505	3.3 CK505	Off[5]	Off[5]	Off[5]	V3.3S	CKPWRGD	
Mobile Intel® 5 Series Chipset	1.05 VCORE	Off[5]	Off[5]	Off[5]	V1.05S		PWROK
WLAN	V3.3A	On	On	On	3.3 V Always		
	M3 Support + Intel® 82577 GbE LAN						
Intel® ME Local RAM	V1.05M	On	Off	Off	V1.05M	SLP_M#[6]	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	On	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	On	Off	Off[7]	V3.3M	SLP_M#[6]	MEPWROK
Integrated LAN controller	VCCLAN	On	Off	Off	V1.05M	SLP_M#[6]	
	No M3 Support + Intel® 82577 GbE LAN						
Intel ME Local RAM	V1.05M	Off	Off	Off	V1.05M	SLP_M#[6]	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	Off	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off[7]	V3.3M	SLP_M#[6]	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	V1.05M	SLP_M#[6]	
	No M3 Support + No Intel® 82577 GbE LAN						
Intel ME Local RAM	V1.05M/1.1M	Off	Off	Off	V1.05M	SLP_M#[6]	MEPWROK
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off[7]	V3.3M	SLP_M#[6]	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	Grounded		

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Title: IBEXPEAK - M (GND)

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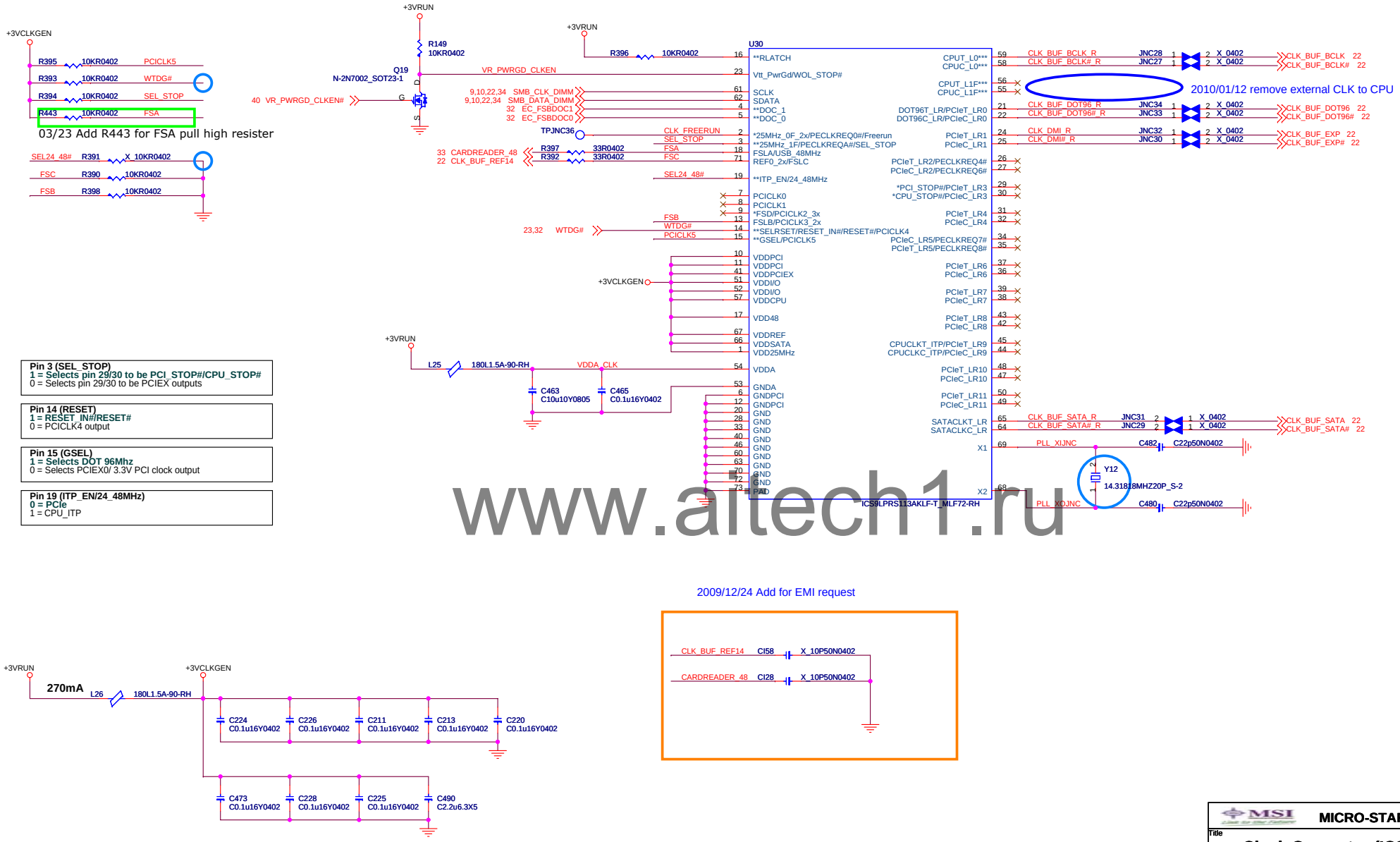

MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator (ICS9LPR113)

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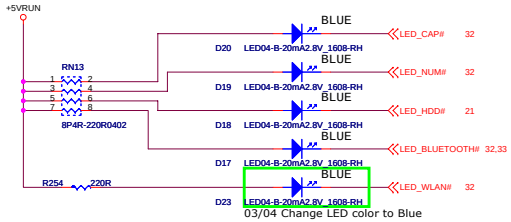
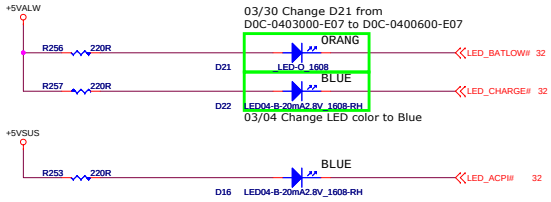
LED

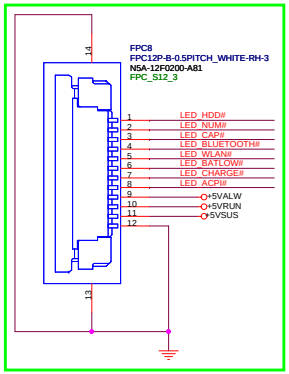


03/04 Change LED color to Blue



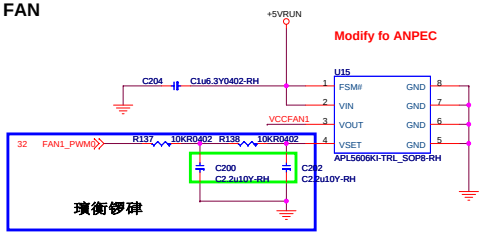
03/30 Change D21 from D0C-0403000-E07 to D0C-0400600-E07

03/04 Change LED color to Blue

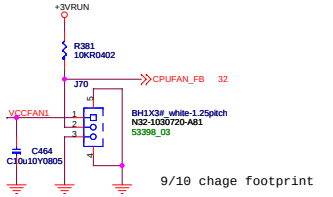


03/25 Move ODM LED Function to MB

CPU FAN

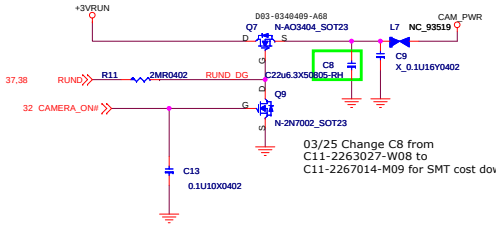


03/25 Change C200.C202 from C11-2253013-Y01 to C11-2253413-W08 for SMT cost down

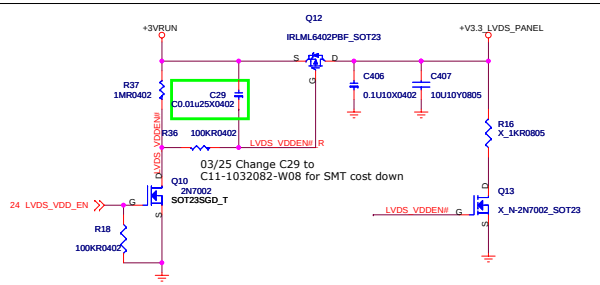


9/10 chage footprint

CAMERA LVDS ON

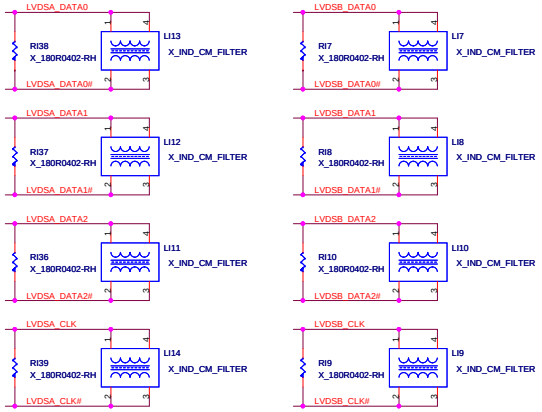


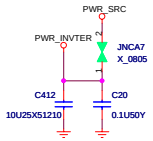
03/25 Change C8 from C11-2263027-W08 to C11-2267014-M09 for SMT cost down



03/25 Change C29 to C11-1032082-W08 for SMT cost down

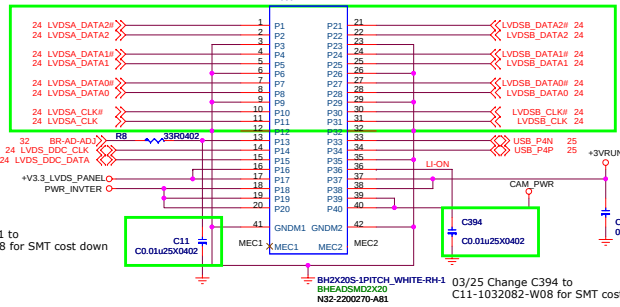
LVDS Connector





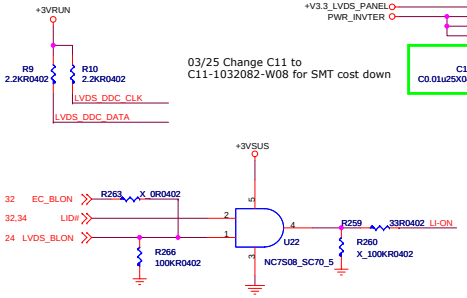
ChA.L ChB.H

Follow MS-16GK Pin define J69



03/25 Change C11 to C11-1032082-W08 for SMT cost down

03/25 Change C394 to C11-1032082-W08 for SMT cost down



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Title: FAN,LED,Lauch board conn

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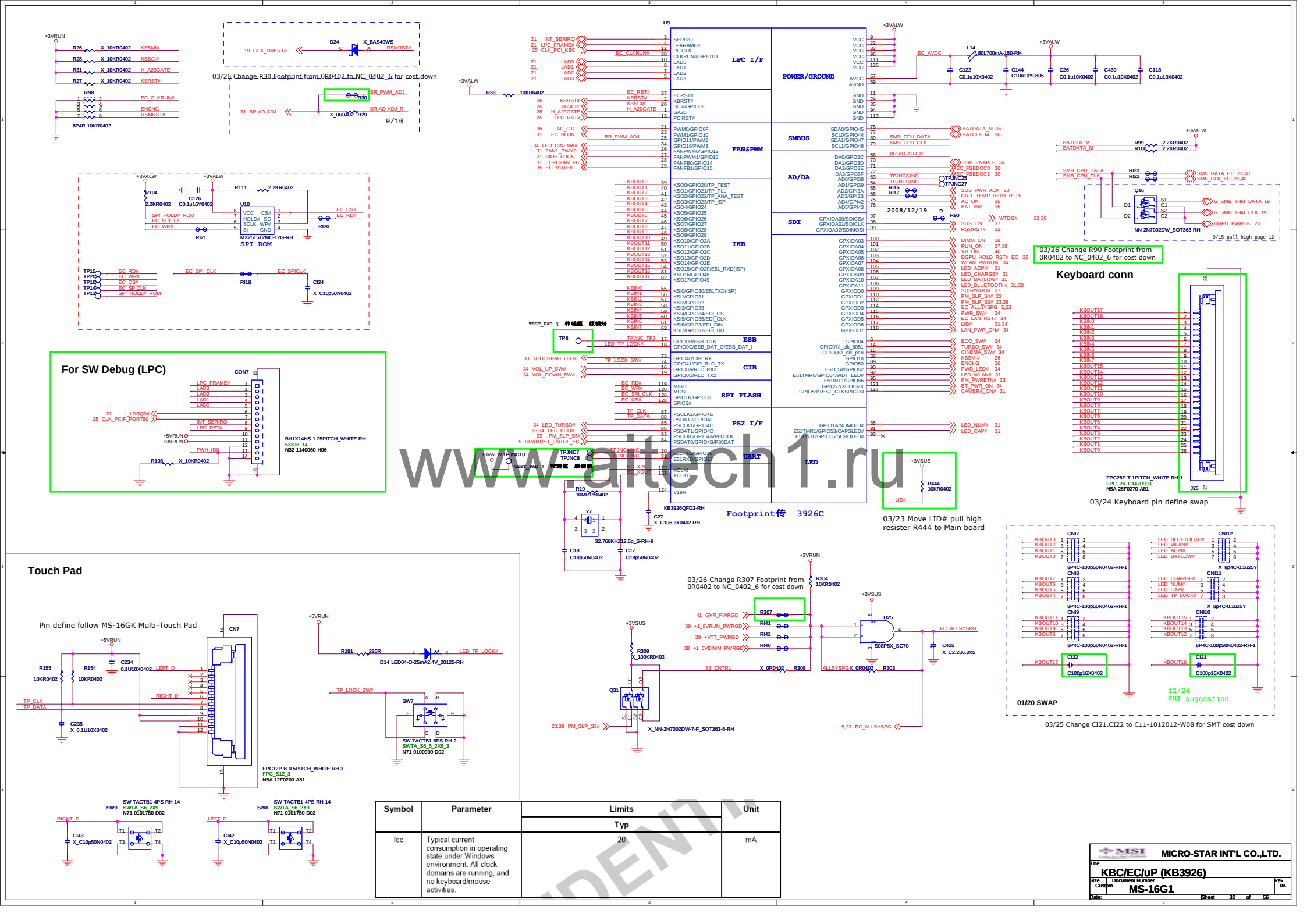

Symbol	Parameter	Limits	Unit
		Typ	
Icc	Typical current consumption in operating state under Windows environment. All clock domains are running, and no keyboard/mouse activities.	20	mA

MICRO-STAR INT'L CO.,LTD.

Title: KBC/EC/uP (KB3926)

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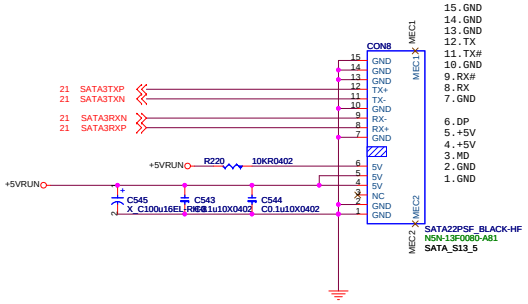
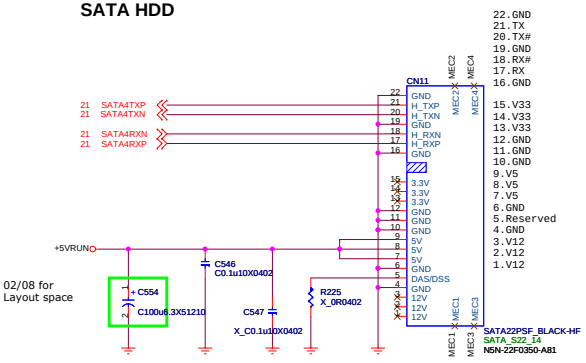
SATA ODD



SATA HDD



02/08 for Layout space

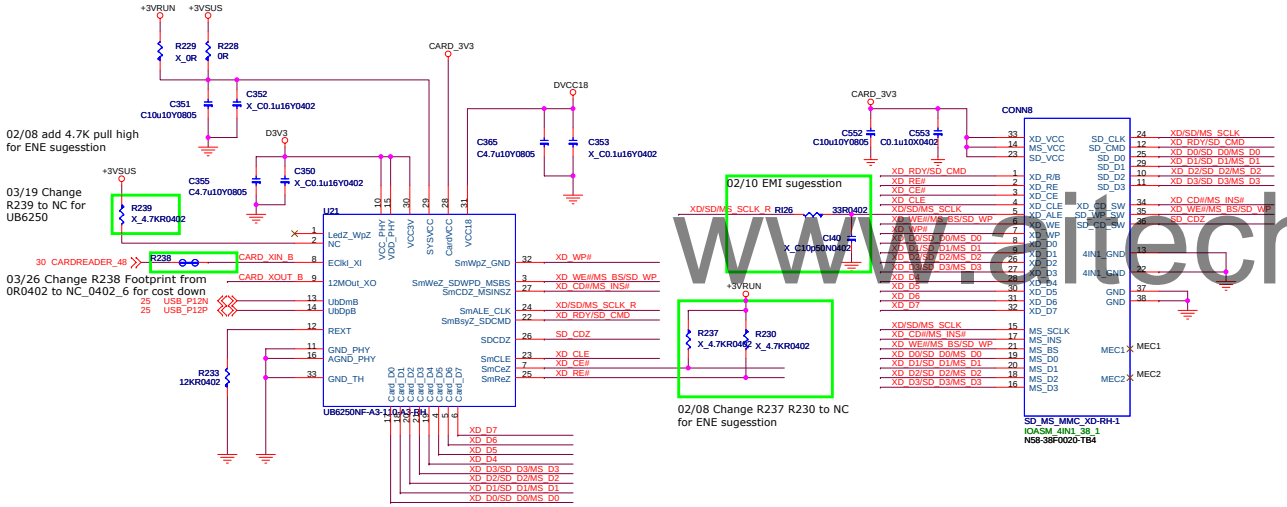
2009/05/15 s for Staggered Spin-up 之崗币笆

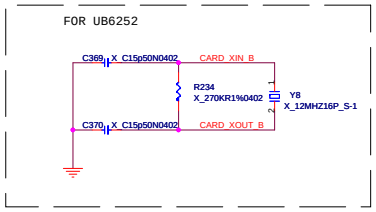
SCREW3 SCREW4
M2X4 E43-1204005-H29
M2X4 E43-1204005-H29

03/30 Add SCREW3.SCREW4 for ME requestion

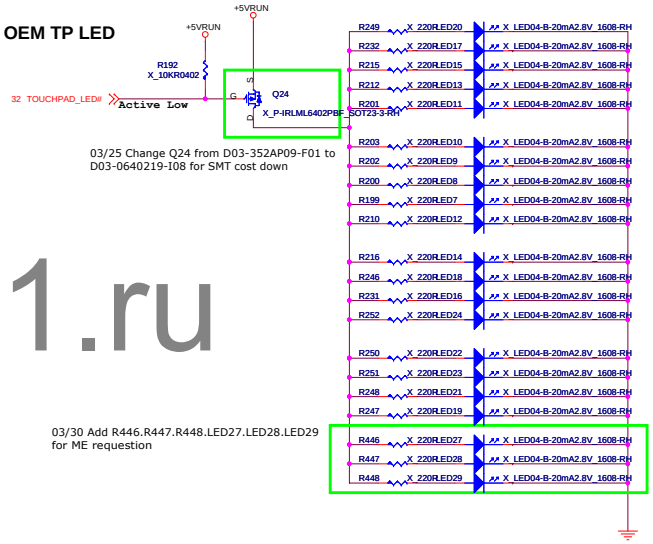
02/02 Remove BT Connector

Card Reader UB6250





OEM TP LED



02/02 Remove LED for match Medion and Channel new rule

MICRO-STAR INT'L CO.,LTD.

Title: ODD HDD Cardreader

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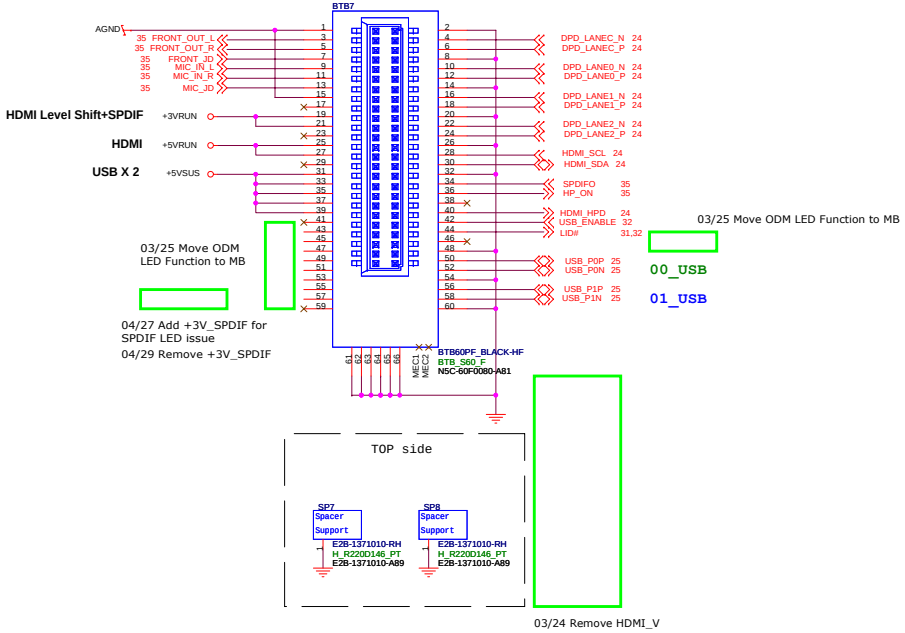
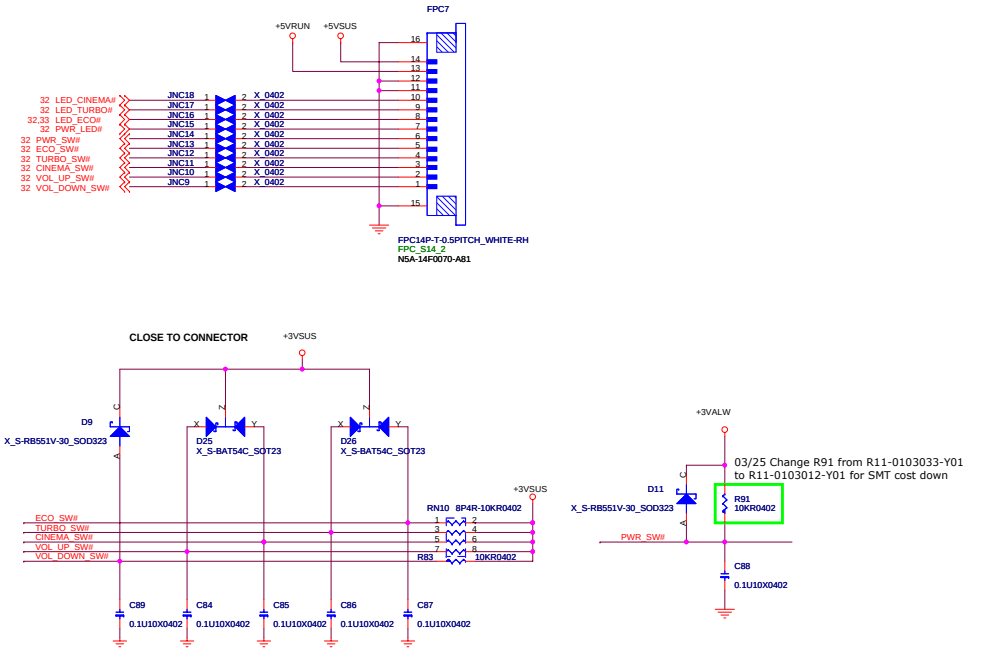
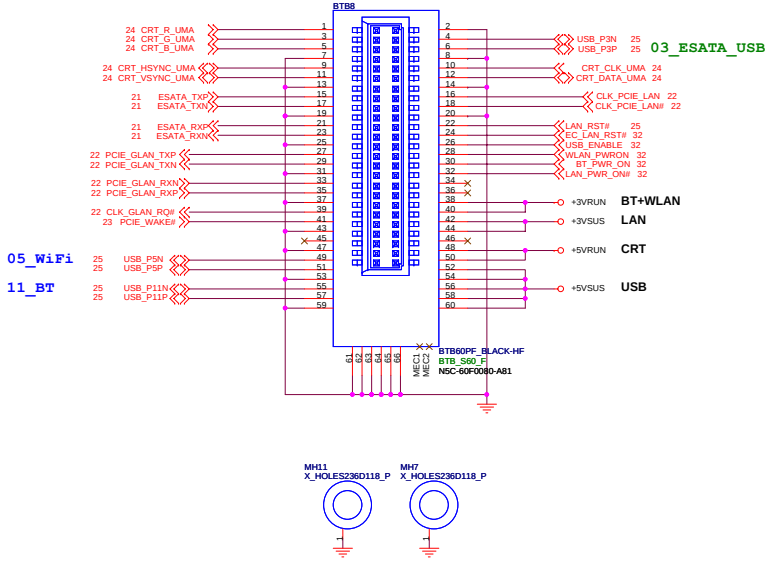
(オ凹HDMI,Audio,USB x 2)

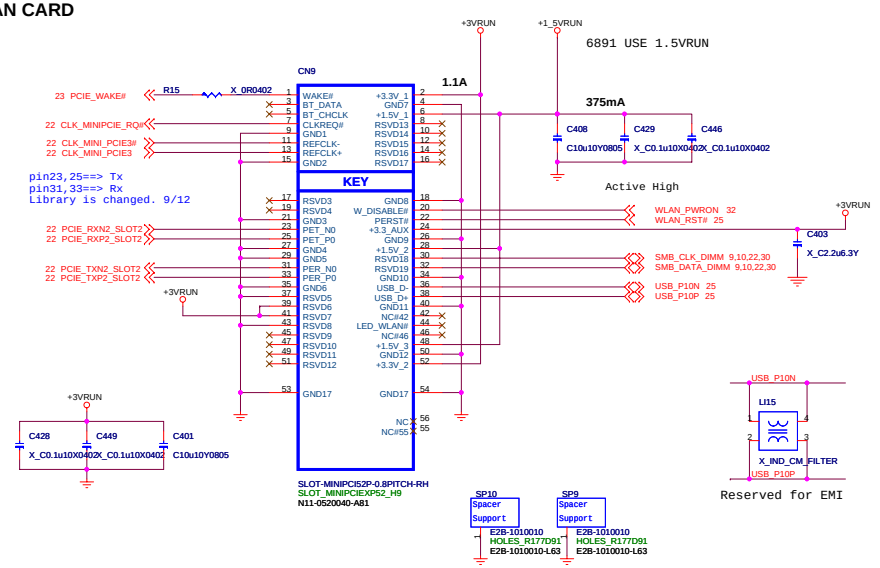




(凹ESATA,USB,LAN,CRT,BT+WLAN)



WLAN CARD



MICRO-STAR INT'L CO.,LTD.

Title: BTB PCIE Connectors

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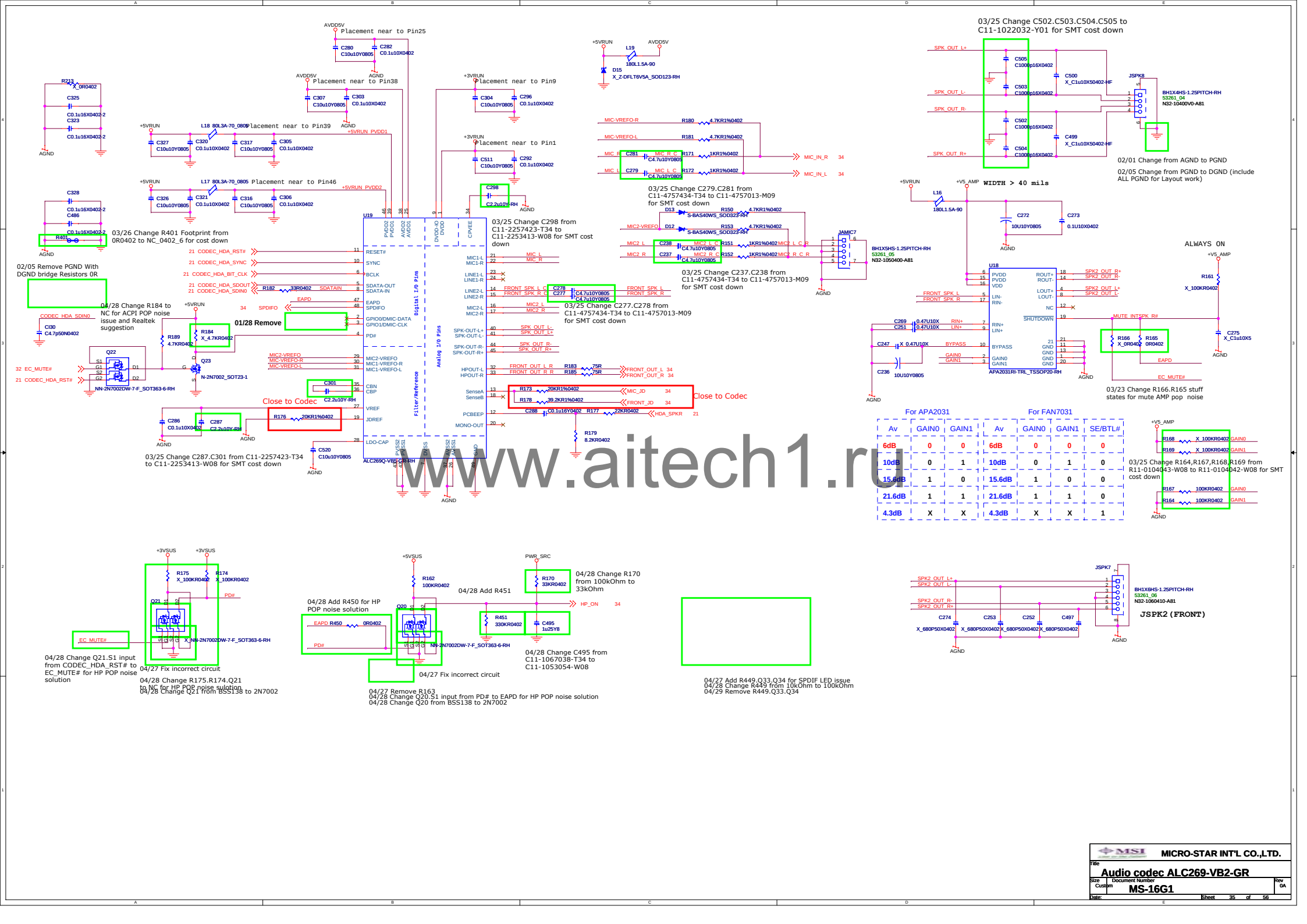
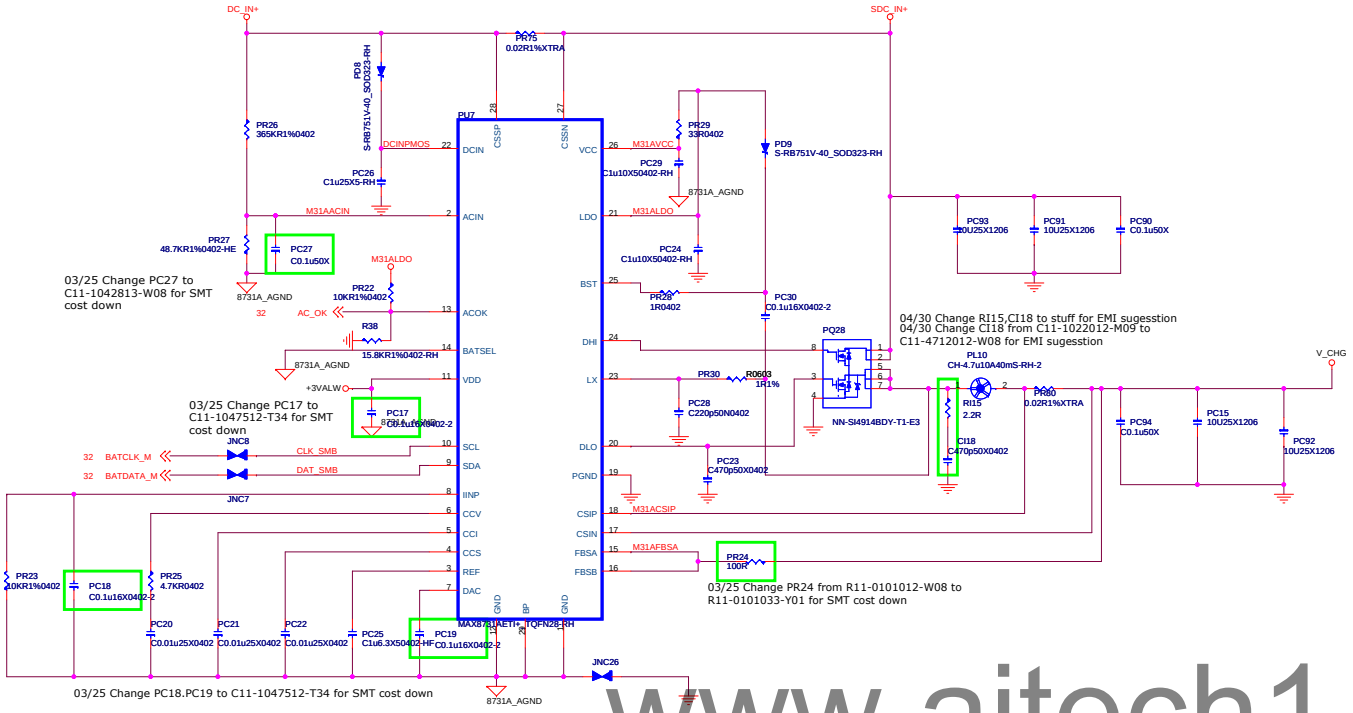


Adapter input voltage set 19 Voltage



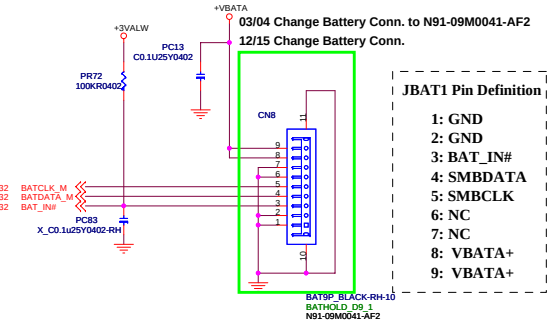
03/25 Change PC27 to C11-1042813-W08 for SMT cost down

03/25 Change PC17 to C11-1047512-T34 for SMT cost down

03/25 Change PC18.PC19 to C11-1047512-T34 for SMT cost down

04/30 Change RI15,CI18 to stuff for EMI sugesstion
04/30 Change CI18 from C11-1022012-M09 to C11-4712012-W08 for EMI sugesstion

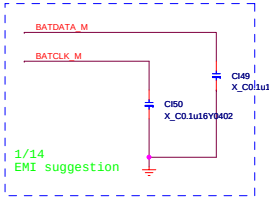
03/25 Change PR24 from R11-0101012-W08 to R11-0101033-Y01 for SMT cost down



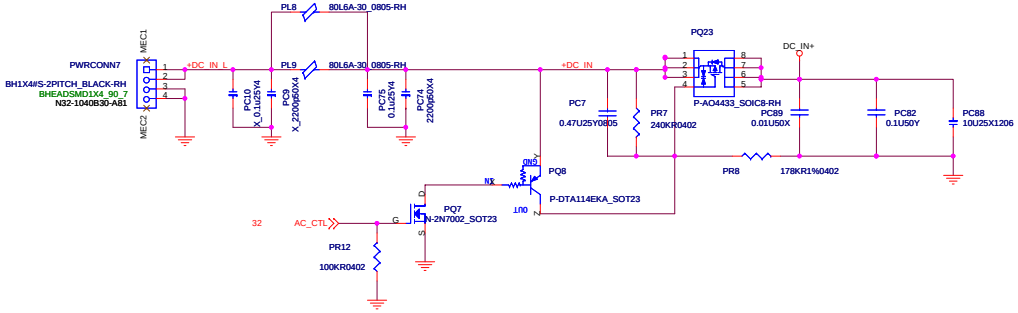
03/04 Change Battery Conn. to N91-09M0041-AF2
12/15 Change Battery Conn.

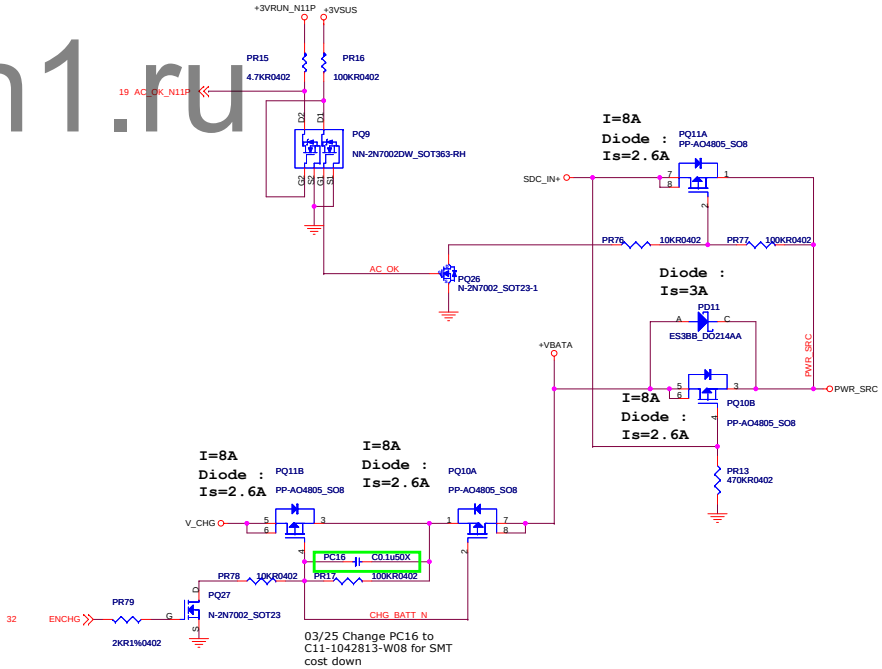
JBAT1 Pin Definition

1: GND
2: GND
3: BAT_IN#
4: SMBDATA
5: SMBCLK
6: NC
7: NC
8: VBATA+
9: VBATA+



IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. V_IINP = IINPUT x RS1 x 3mA/V x PR25





03/25 Change PC16 to C11-1042813-W08 for SMT cost down

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Title: **Battery Select & Charger**

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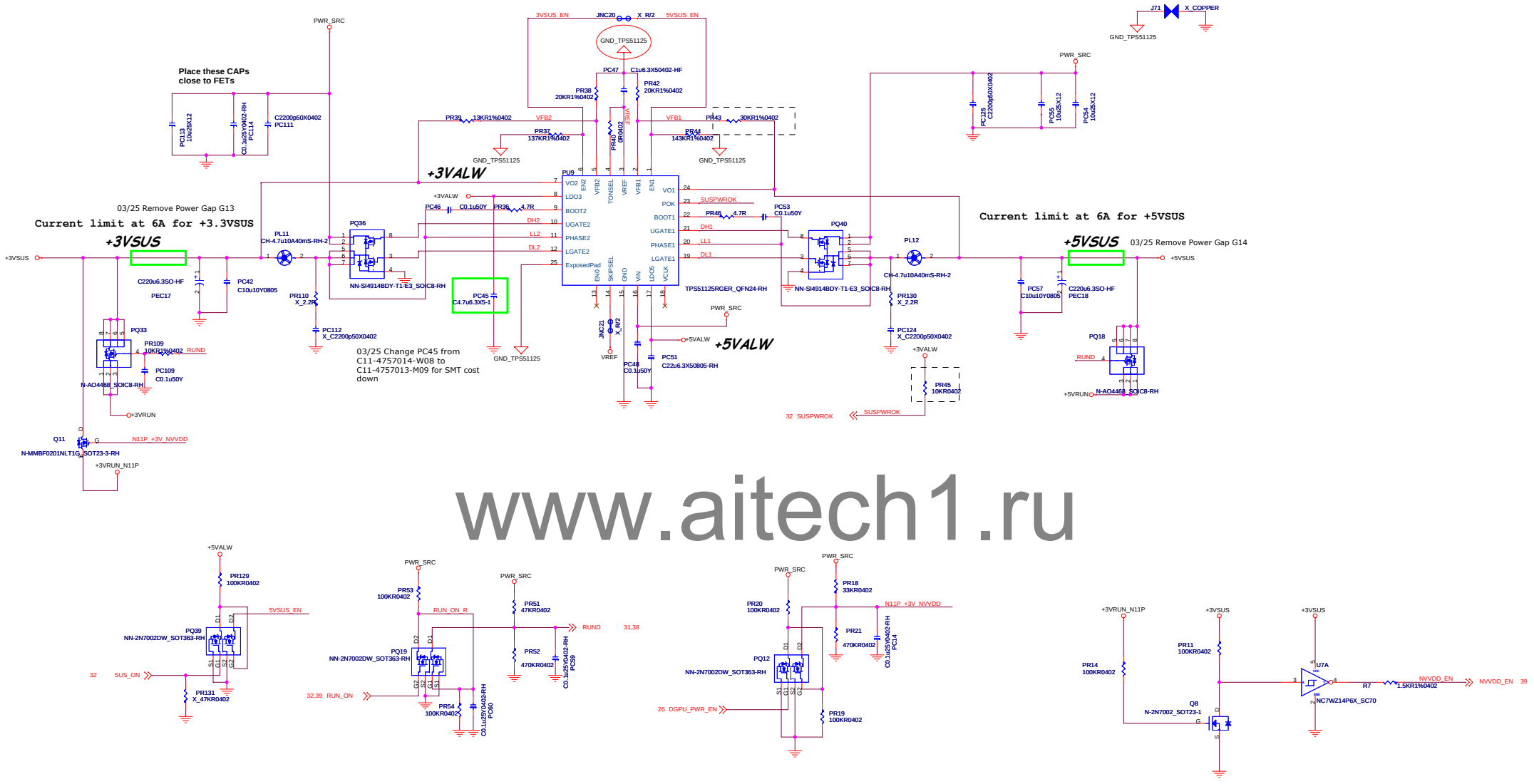

MICRO-STAR INT'L CO.,LTD.

Title: System power

Size: Custom | Document Number: MS-16G1 | Rev: 0A

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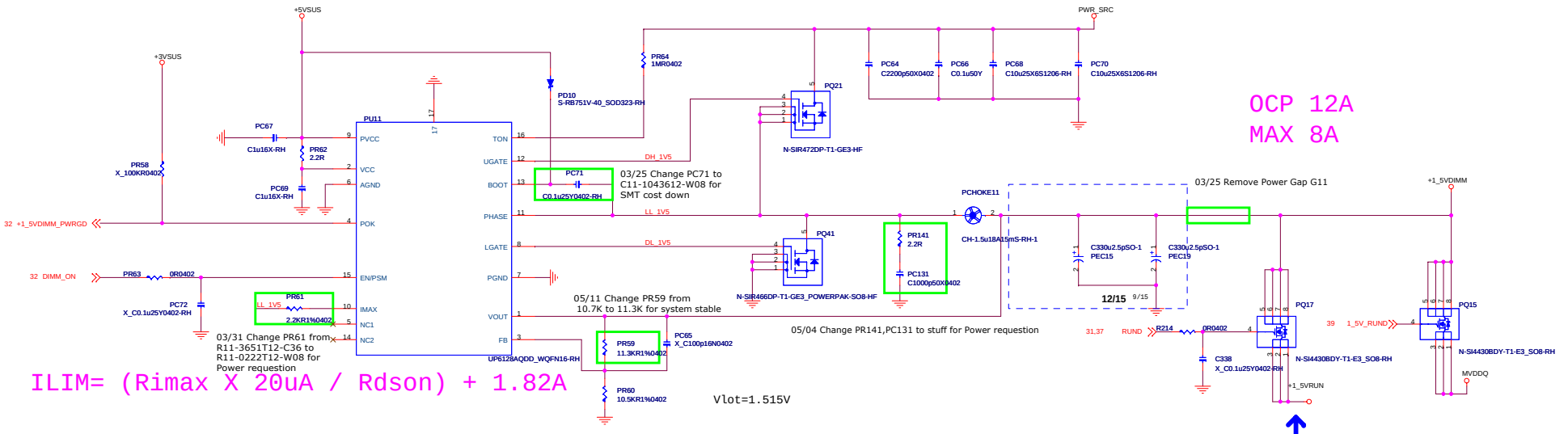
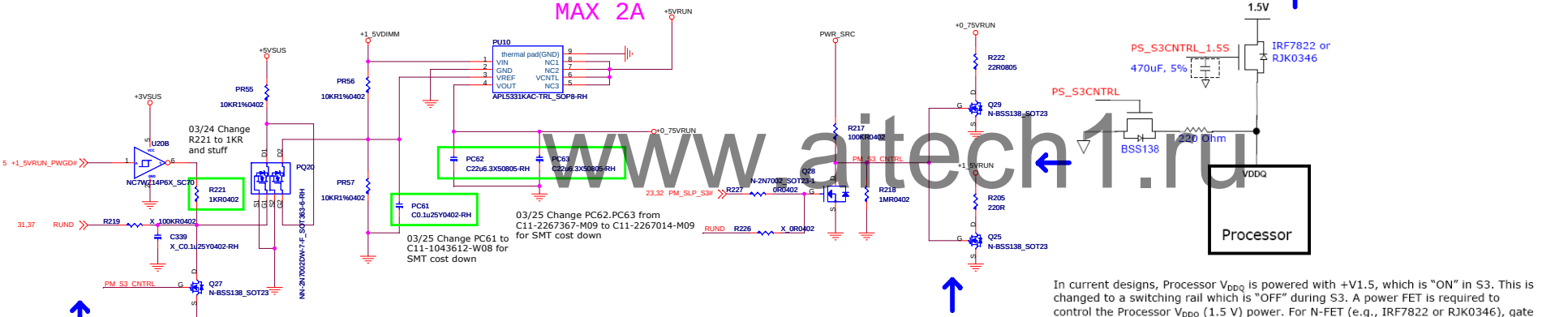
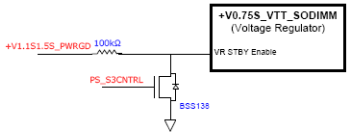
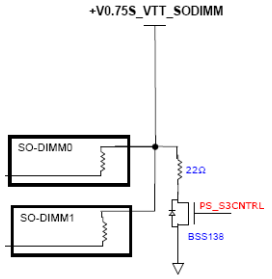






+V0.75S_VTT_DIMM should ramp up later than +V1.5S_CPU_VDDQ. Circuit shown above is used to delay +V0.75V_VTT_SODIMM ramp with respect to +V1.5S_CPU_VDDQ.

100-kΩ isolation resistor is used in reference design so that when gate is turned on, it does not pull +V1.1S1.5S_PWRGD signal to low which may impact other functionality on the board. To ensure +V1.1S1.5S_PWRGD signal levels maintained, comparator pull-up has been changed from 100 kΩ to 1 kΩ (R2F2 in Intel CRB schematic).



CKE is driven low by the processor to put the memory in self refresh while entering S3. When the processor +V1.5_CPU_VDDQ power is turned off, the discharge path on +V0.75S ensures CKE stays low during S3. To avoid any glitch on CKE signals during S3 entry, faster (22 Ω) discharge circuitry ensures +V0.75 ramps down before processor +V1.5S_CPU_VDDQ is turned off.

In current designs, Processor V_{DDQ} is powered with +V1.5, which is "ON" in S3. This is changed to a switching rail which is "OFF" during S3. A power FET is required to control the Processor V_{DDQ} (1.5 V) power. For N-FET (e.g., IRF7822 or RJK0346), gate voltage of FET (PS_S3CNTRL_1.5S) is derived from SLP_S3# and at 12-V logic. RDS(ON) of the FET used in CRB is in the range of 5 mΩ. Every design is different and designer should select an appropriate FET so that the required voltage rail specification is maintained at the Processor V_{DDQ} pins.

Signal Name	Source	Voltage Level	Comments
PS_S3CNTRL	Inverted SLP_S3# signal	In CRB, it is a 3.3-V signal.	Voltage should be high enough to turn ON or OFF the MOSFET. When selecting the MOSFET, insure $V_{gs}>V_{gsth}$.
PS_S3CNTRL_1.5S	Buffered SLP_S3# signal	In Intel CRB it is a 12-V signal.	Voltage should be high enough to turn ON or OFF the Power MOSFET. When selecting the MOSFET, insuree $V_{gs}>V_{gsth}$.

MICRO-STAR INT'L CO.,LTD.

Title: SMDDR_VTERM /1_5VRUN

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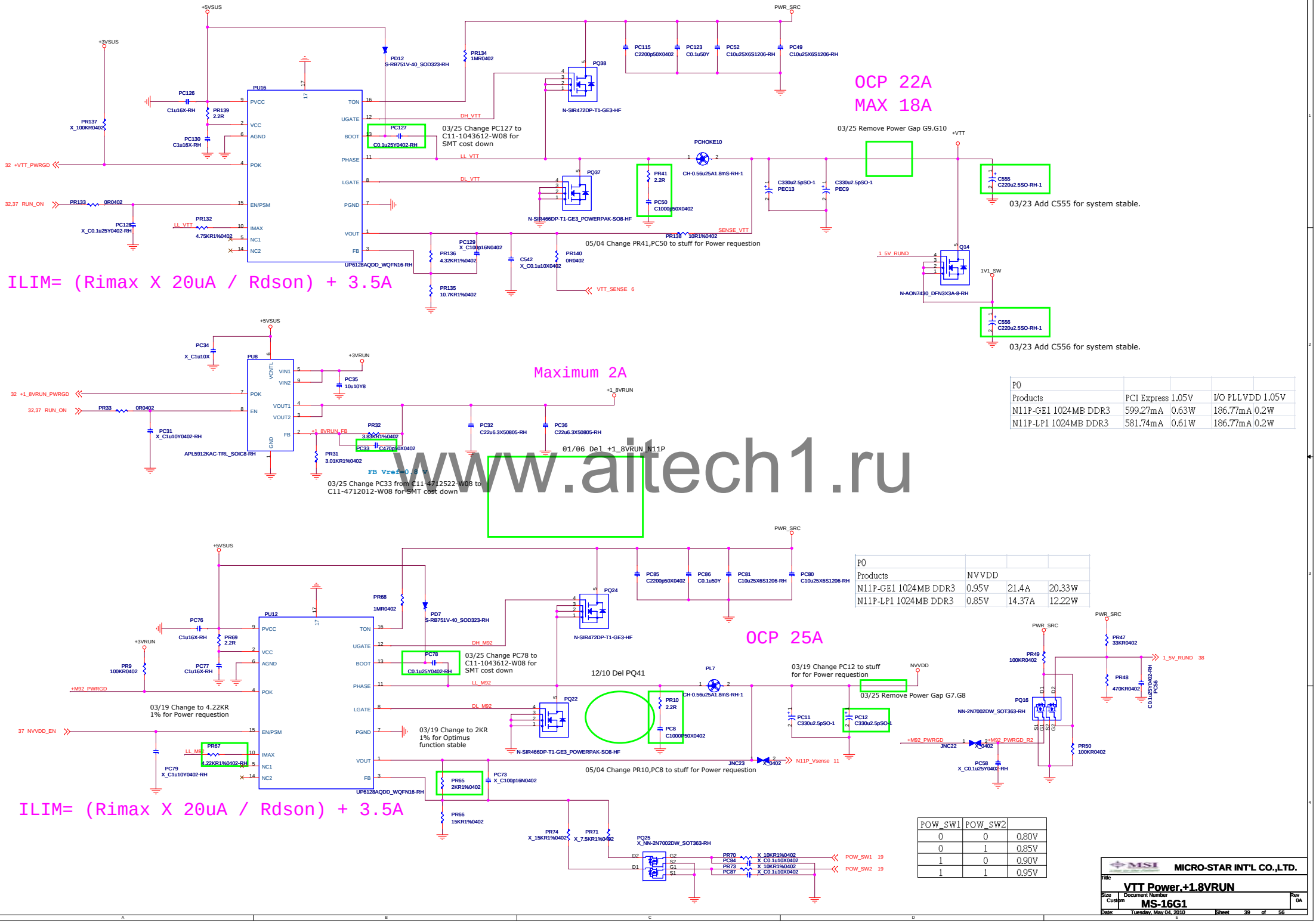

P0			
Products	PCI Express 1.05V		I/O PLLVDD 1.05V
N11P-GE1 1024MB DDR3	599.27mA	0.63W	186.77mA 0.2W
N11P-LP1 1024MB DDR3	581.74mA	0.61W	186.77mA 0.2W

P0			
Products	NVVDD		
N11P-GE1 1024MB DDR3	0.95V	21.4A	20.33W
N11P-LP1 1024MB DDR3	0.85V	14.37A	12.22W

POW_SW1	POW_SW2	
0	0	0.80V
0	1	0.85V
1	0	0.90V
1	1	0.95V

MICRO-STAR INT'L CO.,LTD.

Title: VTT Power,+1.8VRUN

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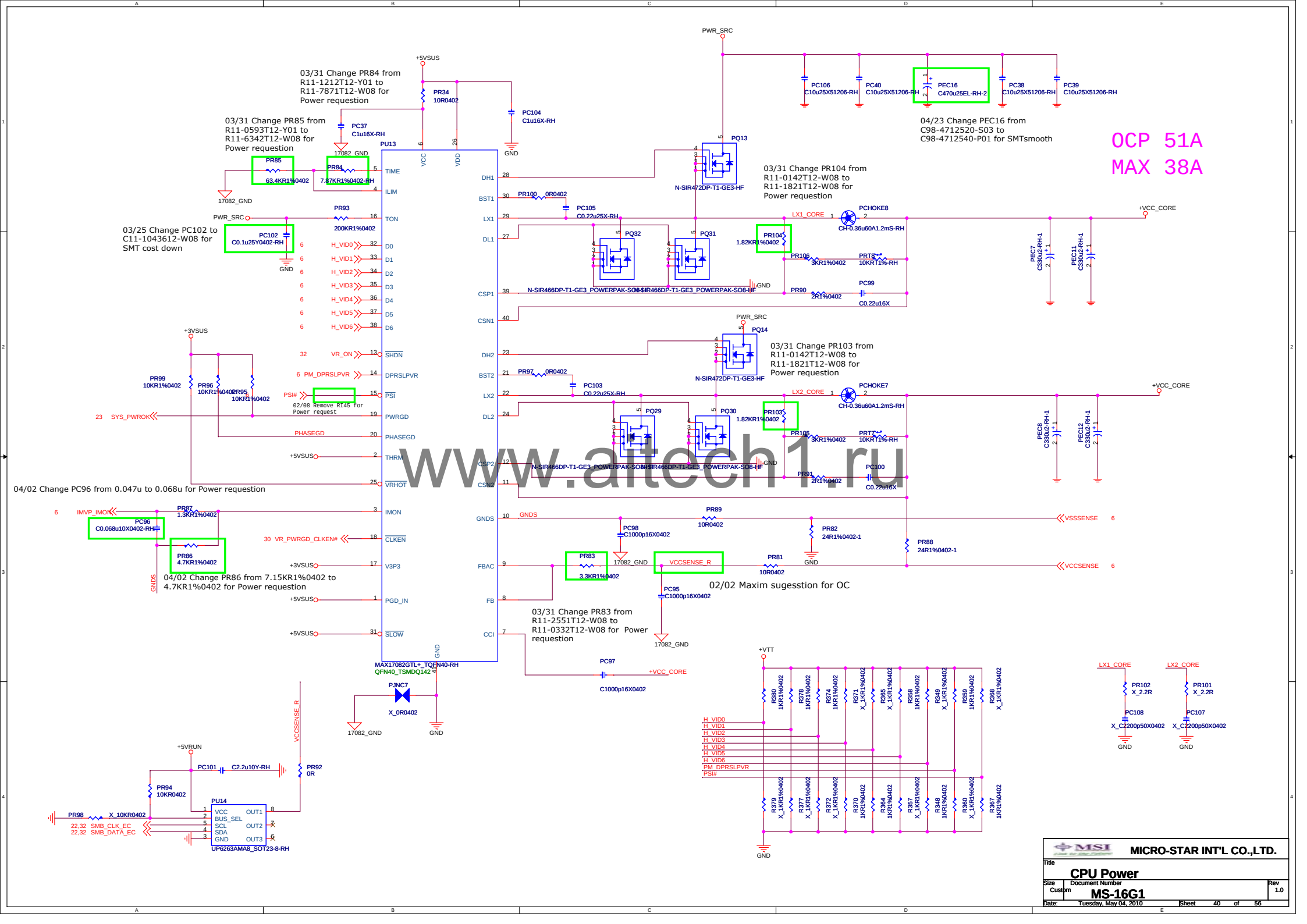
03/31 Change PR84 from R11-1212T12-Y01 to R11-7871T12-W08 for Power requestion
03/31 Change PR85 from R11-0593T12-Y01 to R11-6342T12-W08 for Power requestion
03/25 Change PC102 to C11-1043612-W08 for SMT cost down
04/02 Change PC96 from 0.047u to 0.068u for Power requestion
04/02 Change PR86 from 7.15KR1%0402 to 4.7KR1%0402 for Power requestion
02/08 Remove R145 for Power request
03/31 Change PR83 from R11-2551T12-W08 to R11-0332T12-W08 for Power requestion
03/31 Change PR104 from R11-0142T12-W08 to R11-1821T12-W08 for Power requestion
03/31 Change PR103 from R11-0142T12-W08 to R11-1821T12-W08 for Power requestion
04/23 Change PEC16 from C98-4712520-S03 to C98-4712540-P01 for SMTsmooth
02/02 Maxim sugesstion for OC
OCP 51A
MAX 38A
MAX17082GTL+_TQFN40-RH
QFN40_TSMDQ142
UP6263AMA8_SOT23-8-RH
N-SIR472DP-T1-GE3-HF
N-SIR466DP-T1-GE3_POWERPAK-SO8-HF
CH-0.36u60A1.2mS-RH
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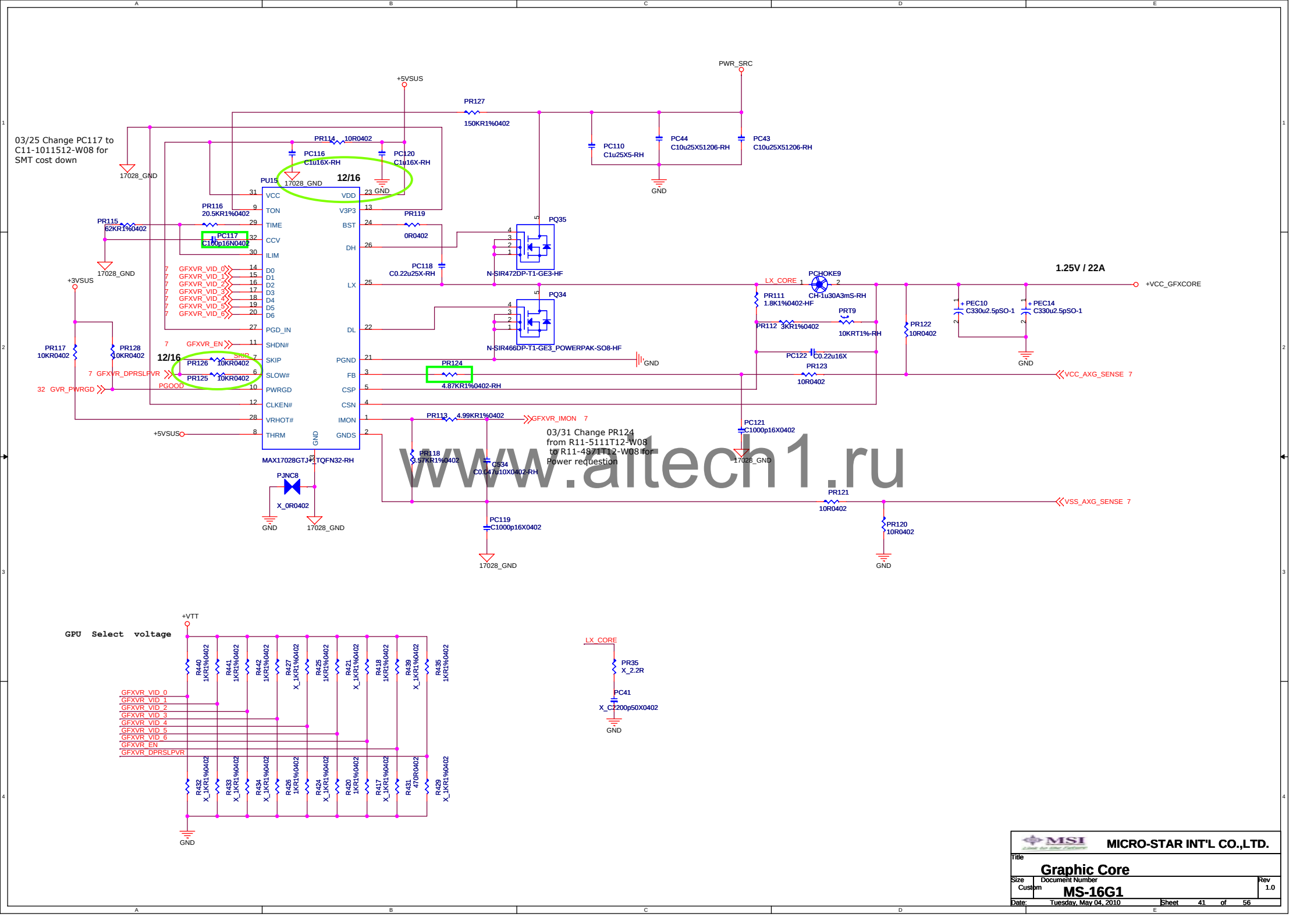
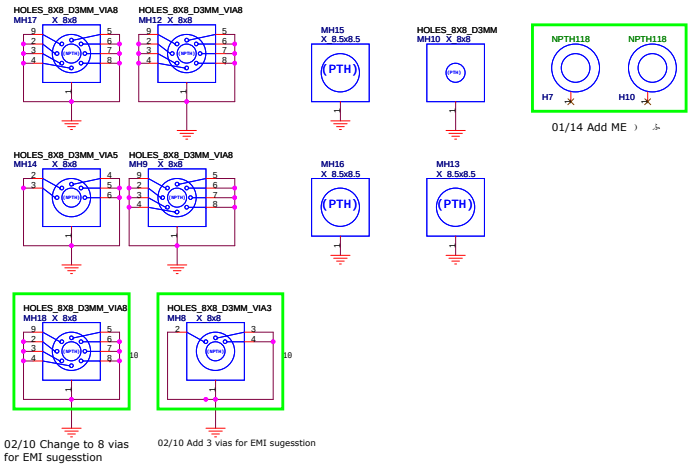
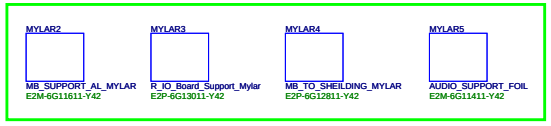
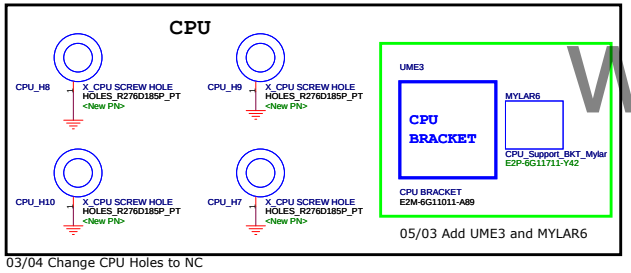




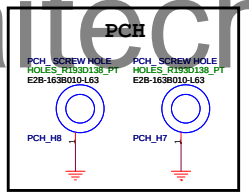


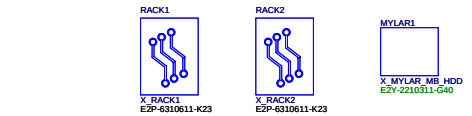
04/23 Add MYLAR2.MYLAR3.MYLAR4.MYLAR5 for ME request

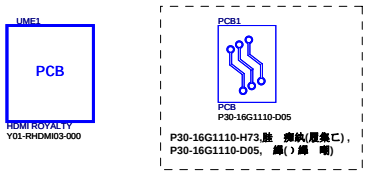


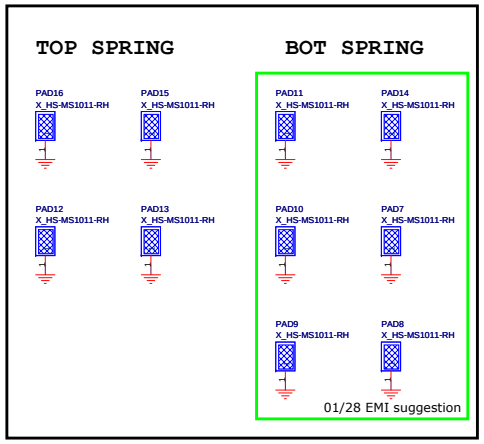
05/03 Add UME3 and MYLAR6

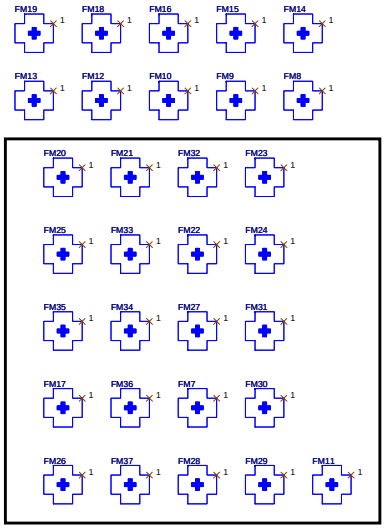
03/04 Change CPU Holes to NC

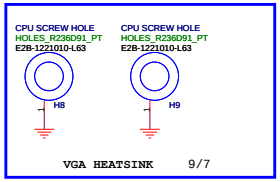


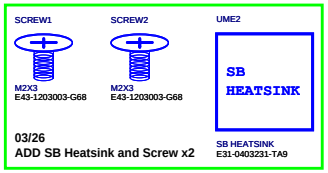












MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME

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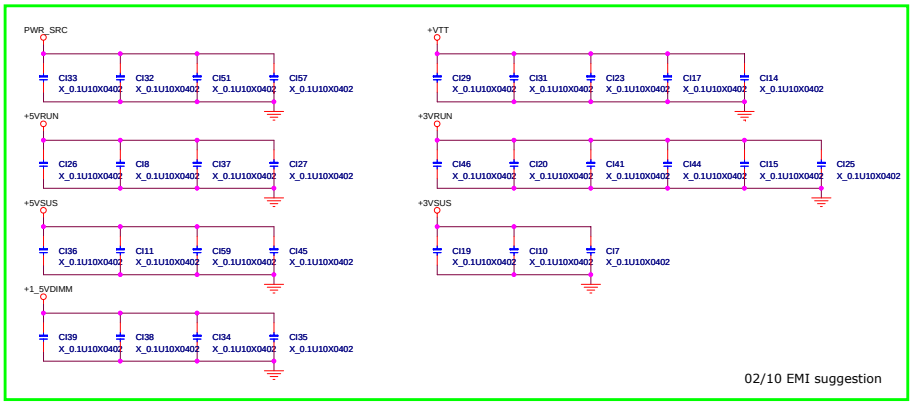

MICRO-STAR INT'L CO.,LTD.

Title: EMI

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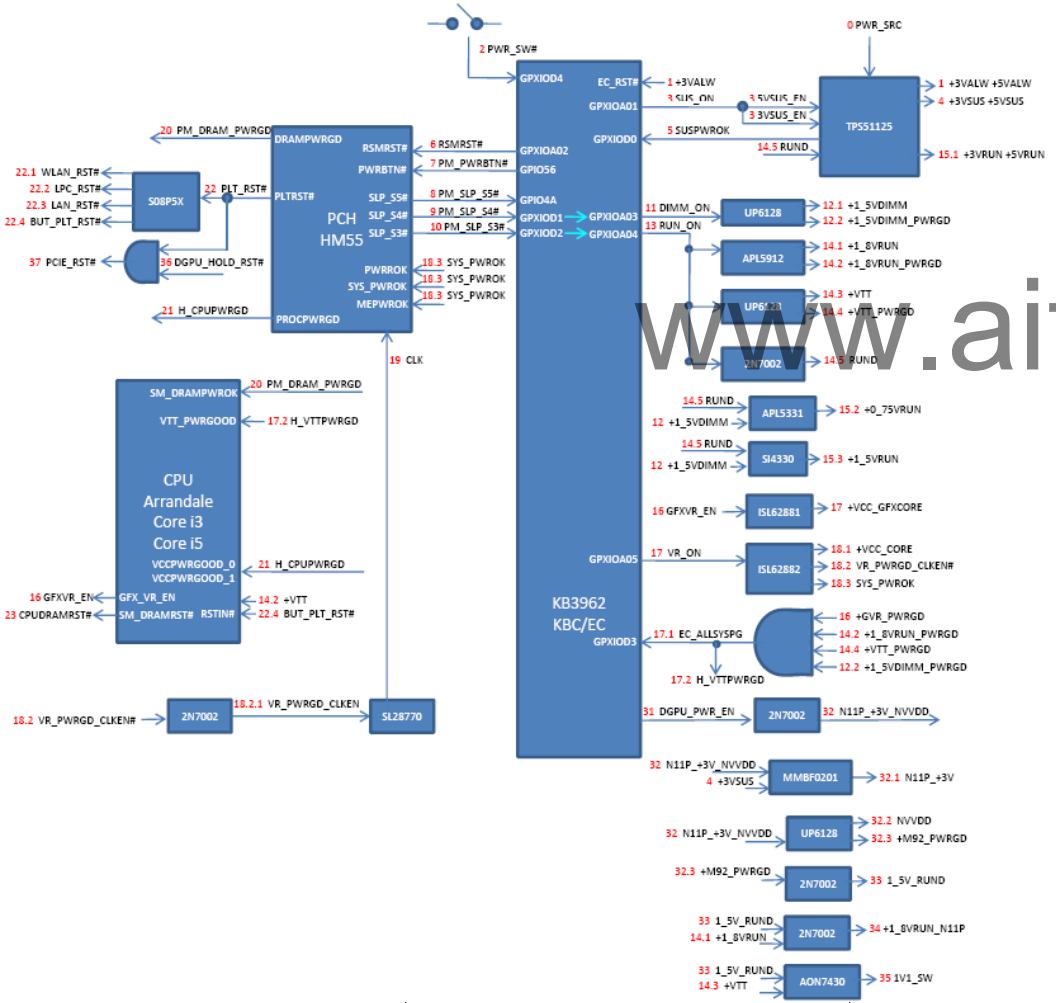
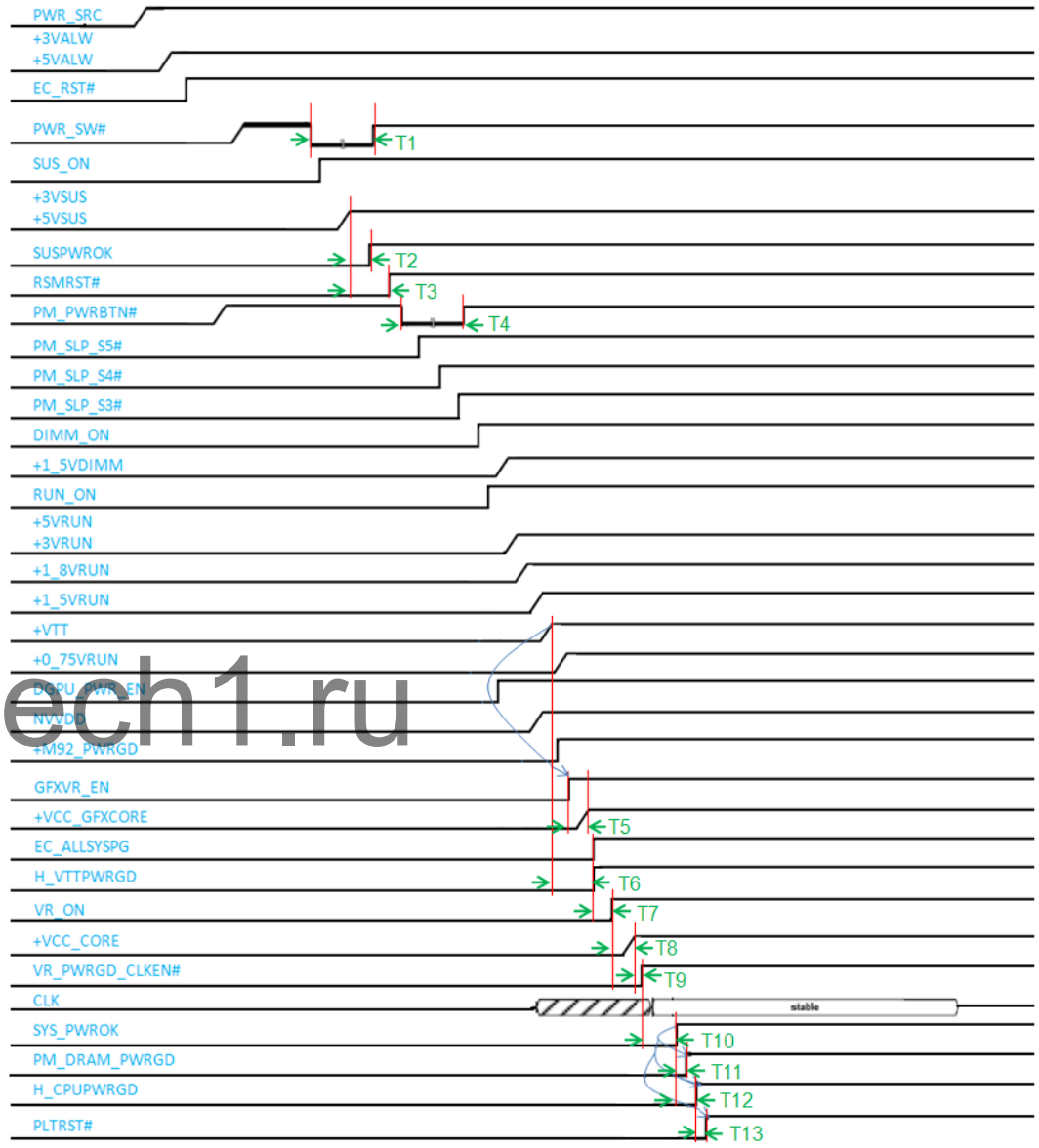
Label	Min	Max	Units	Description
T1	150		ms	
T2	2	2.5	ms	The powergood function is activated with 2 ms internal delay after SUSPWROK goes high. If the output voltage becomes within +/-5% of the target value, PGOOD goes high around 2.5 ms after SUSPWROK goes high.
T3	10		ms	Vcc_SUS stable to RSMRST# deassertion.
T4	150		ms	
T5		1	us	CPU will drive Gfx_VR_EN when VTT ramps. Gfx_VR_EN to Gfx_VID stable. Timing set by Processor.
T6		500	ms	VTT stable to VTTPWRGOOD assertion to the processor.
T7	99		ms	ALL_SYS_PWRGD assertion to IMVP_VR_EN. This timing is generated by EC.
T8		3	ms	
T9	10	100	us	
T10	3	20	ms	IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
T11	1		ms	SYS_PWROK/PCH_PWROK assertion to DRAMPWROK assertion. Timing set by PCH.
T12	1		ms	SYS_PWROK/PCH_PWROK assertion to VCCPWRGOOD0/VCCPWRGOOD_1 assertion. Timing set by PCH.
T13	1		ms	VCCPWRGOOD_0/VCCPWRGOOD_1 assertion to PLTRST# deassertion





MSI MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequency

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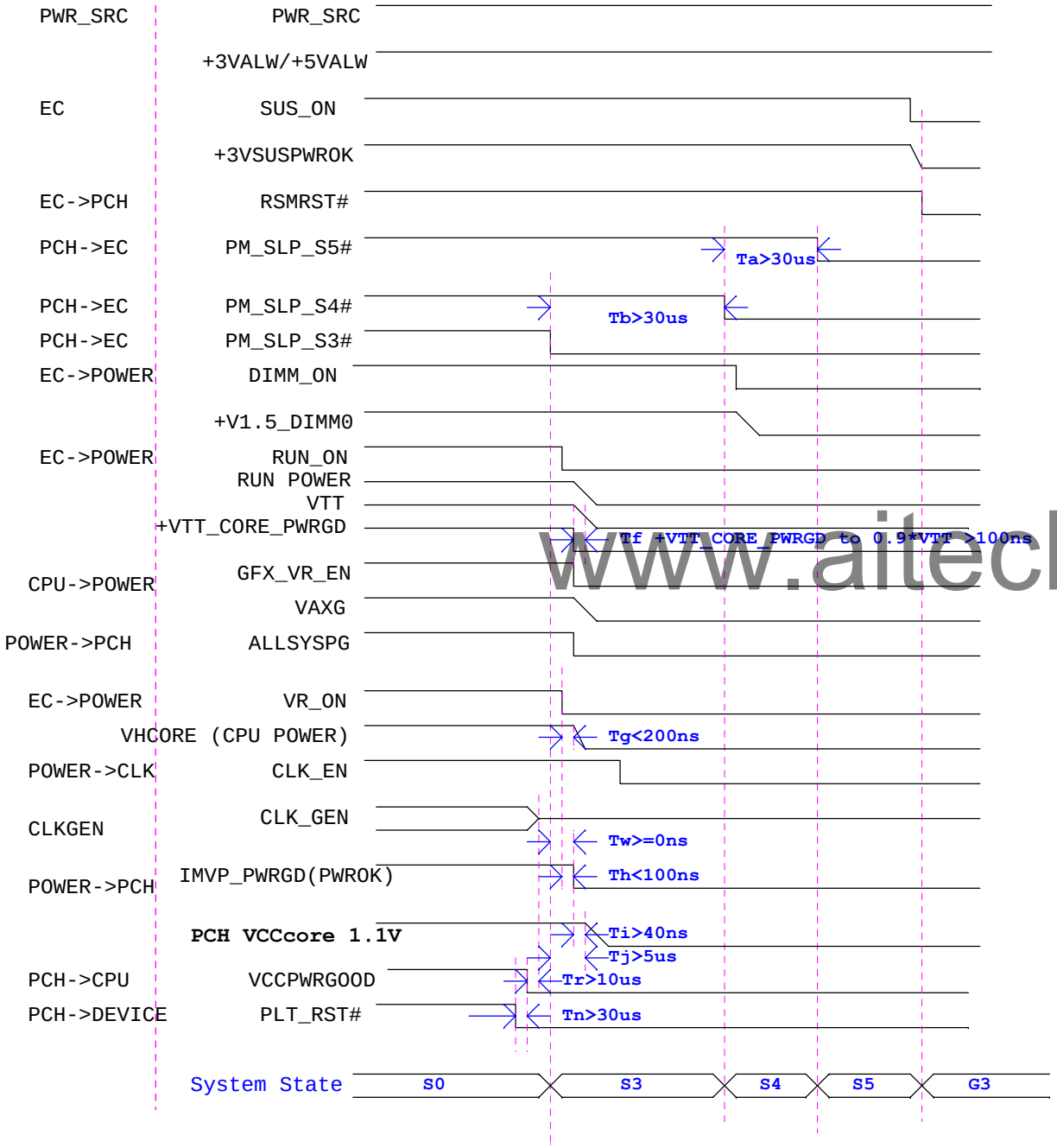
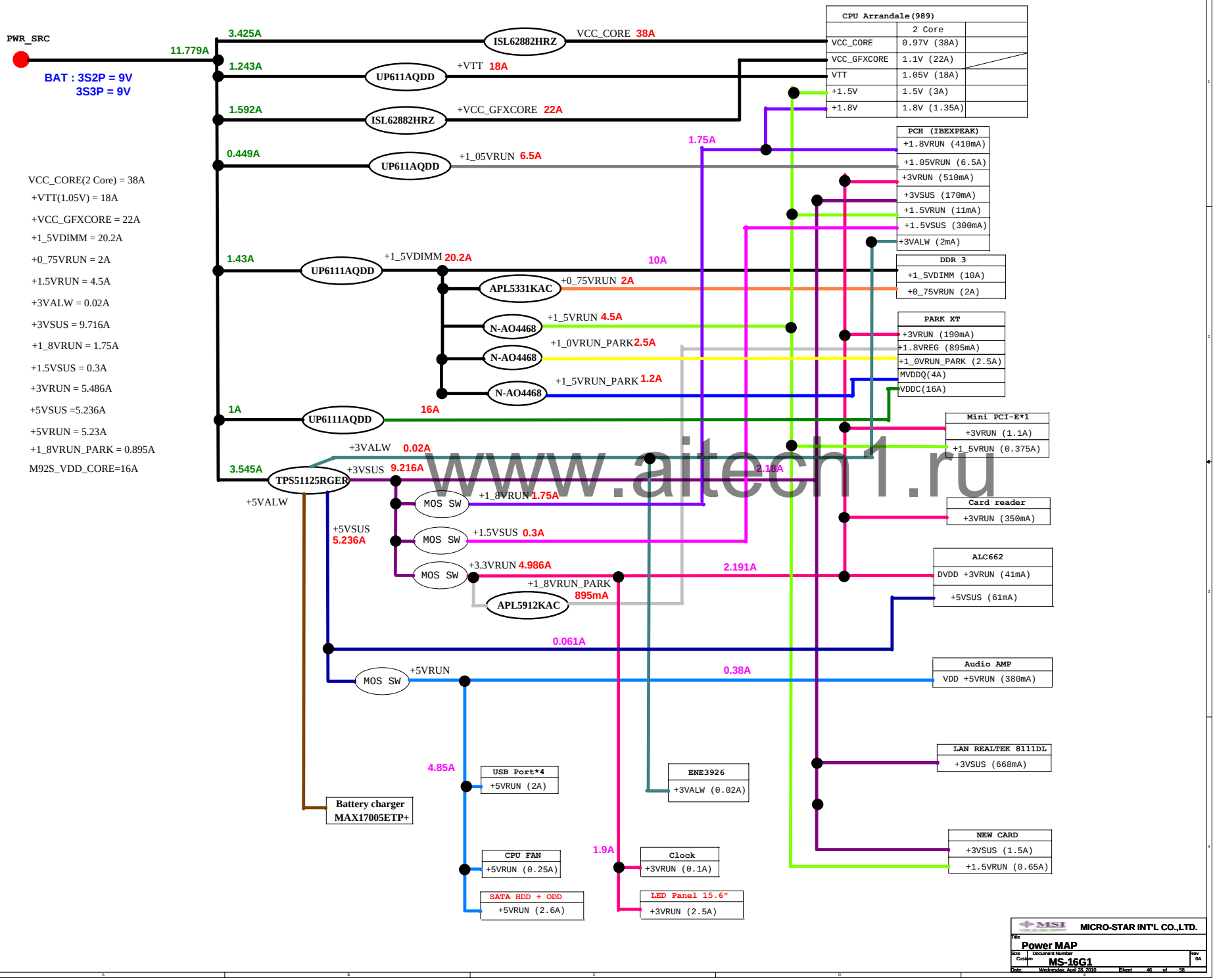
Power down Sequence DC mode S0 to G3



MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequency		
Size: A3	Document Number: MS-16G1	Rev: 0A
Date: Wednesday, April 28, 2010	Sheet 45 of 56	



VCC_CORE(2 Core) = 38A
+VTT(1.05V) = 18A
+VCC_GFXCORE = 22A
+1_5VDIMM = 20.2A
+0_75VRUN = 2A
+1.5VRUN = 4.5A
+3VALW = 0.02A
+3VSUS = 9.716A
+1_8VRUN = 1.75A
+1.5VSUS = 0.3A
+3VRUN = 5.486A
+5VSUS =5.236A
+5VRUN = 5.23A
+1_8VRUN_PARK = 0.895A
M92S_VDD_CORE=16A

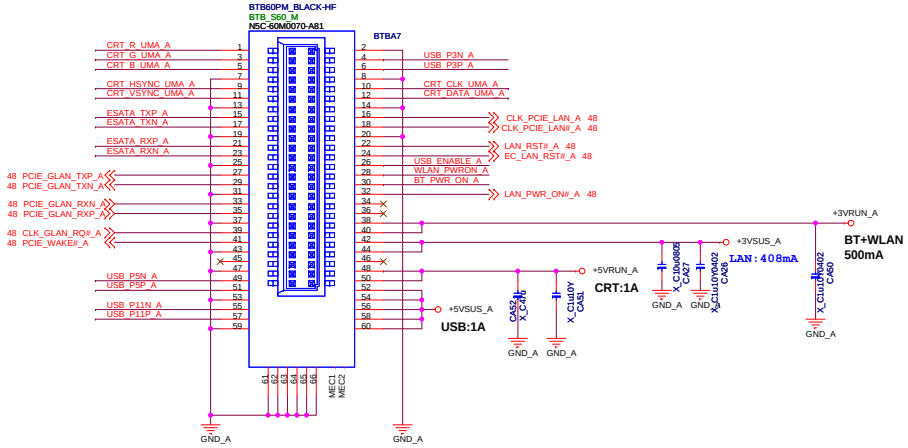
MICRO-STAR INT'L CO.,LTD.

Power MAP

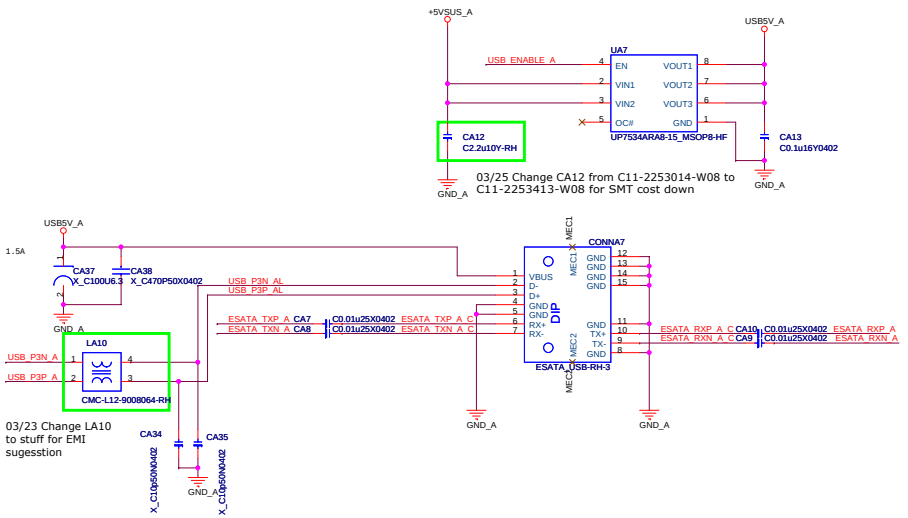
MS-16G1

Wednesday, April 28, 2010

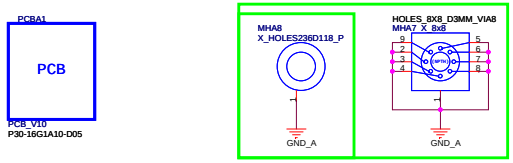
(凹ESATA,USB,LAN,CRT,BT+WLAN)



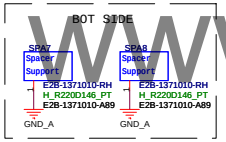
ESATA Connector



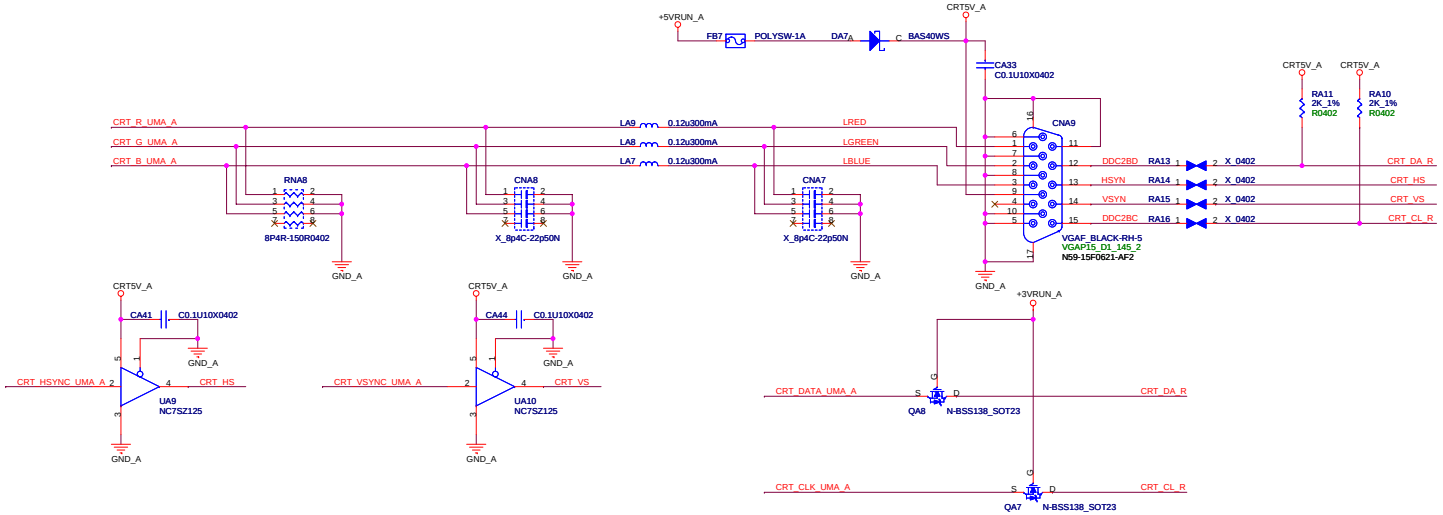
02/25 Change MHA8 to HOLES_R276D185P_PT
03/30 Change MHA8 to HOLES236D118_P



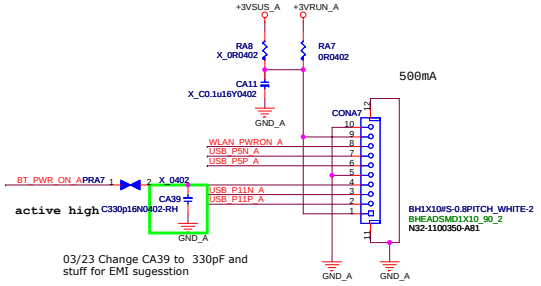
02/23 Change to 8 vias for EMI sugesstion



D-Sub Connecor



BT and WLAN Combo Connector



MSI	MICRO-STAR INT'L CO.,LTD.
Title	CRT/USB/LAN/BT/Conn
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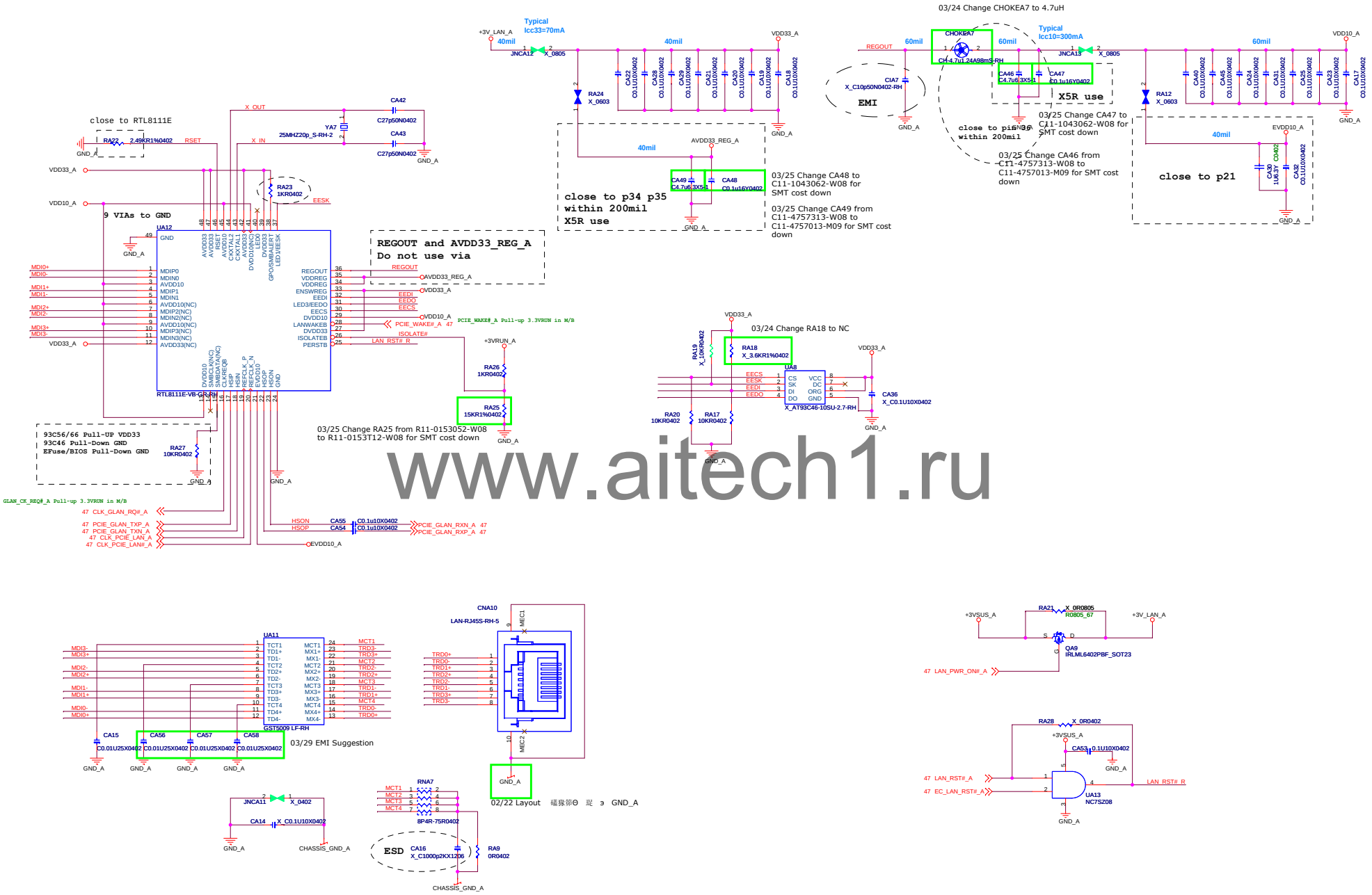

MICRO-STAR INT'L CO.,LTD.

Title: Power MAP

Size: Custom | Document Number: MS-16G1 | Rev: 0A

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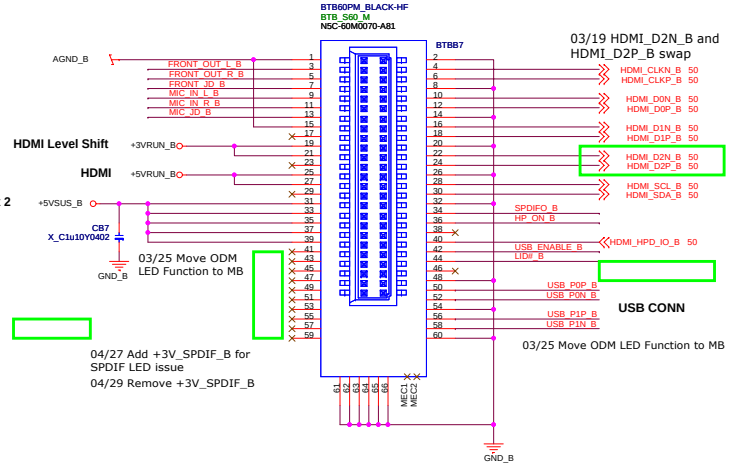
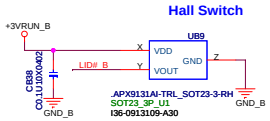
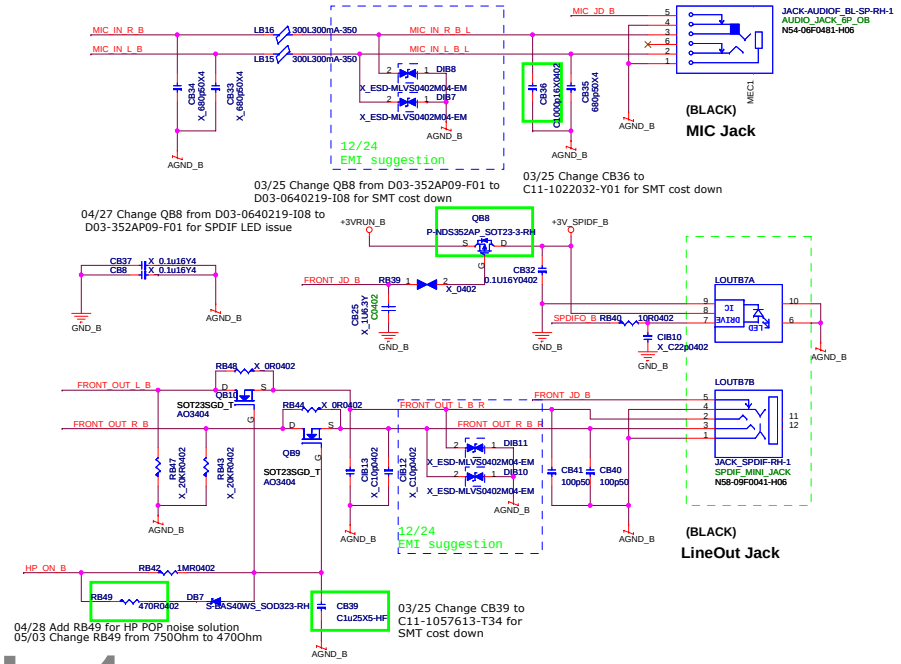
(オ凹HDMI,Audio,USB x 2)



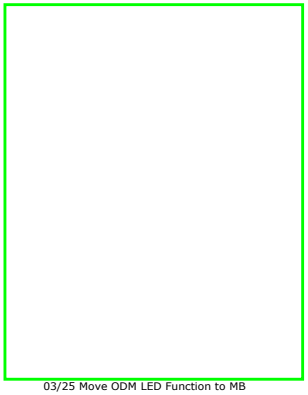
LID Switch



Audio Jack

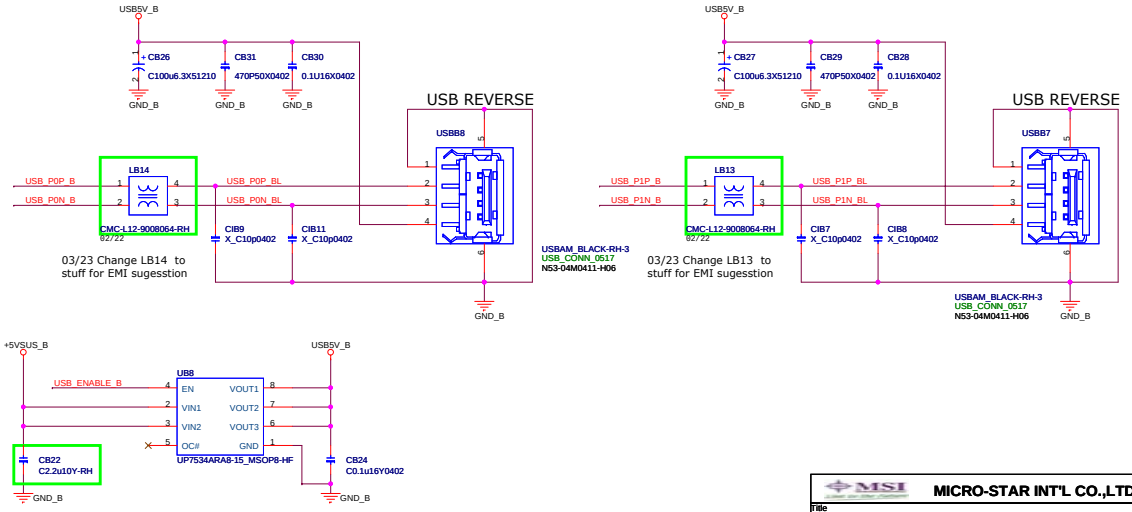


For ODM LED Function



03/25 Move ODM LED Function to MB

USB 2.0 Connector



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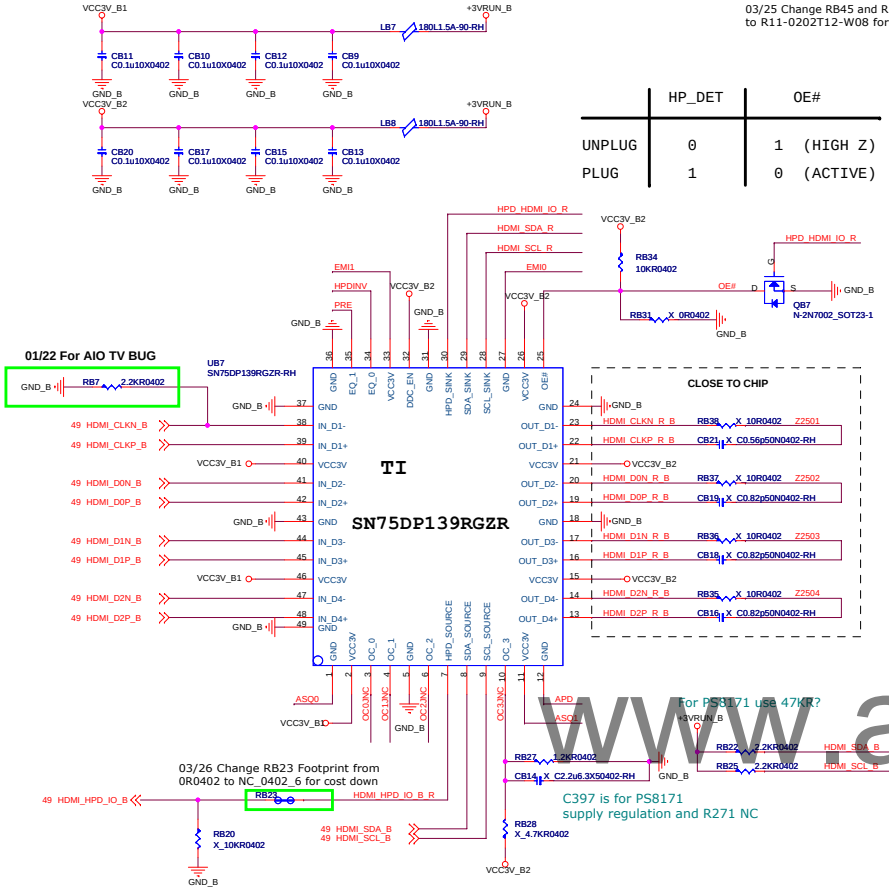
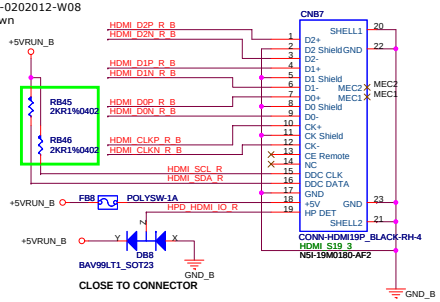
HDMI Level Shift



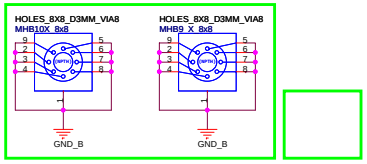
HDMI Connector

03/25 Change RB45 and RB46 from R11-0202012-W08 to R11-0202T12-W08 for SMT cost down



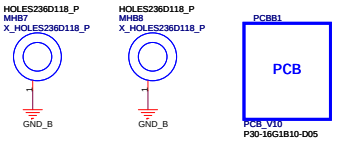
SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500K) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down~500k) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.9V	Pin 4
GND VCC	[ASQ1,ASQ0] = HL: No automatic squelch (Internal pull down~500k) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.65K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up~500k) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND VCC	EMI reduction and filter setting. (EMI1 internal pull up~500K ; EMI0 internal pull down~500K) [EMI1,EMI0] = HL: No EMI reduction EMI0 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (internal pull-down~500K) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500K) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

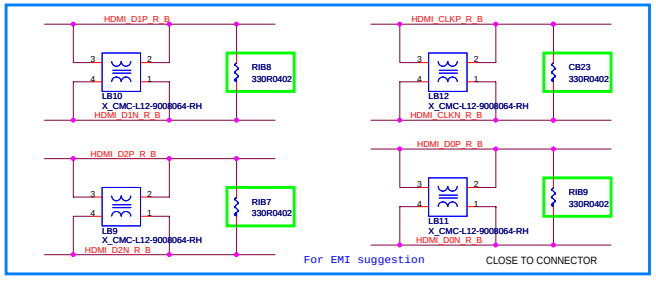
Note2: High is HPD logic inverted, Low is HPD logic non-inverted



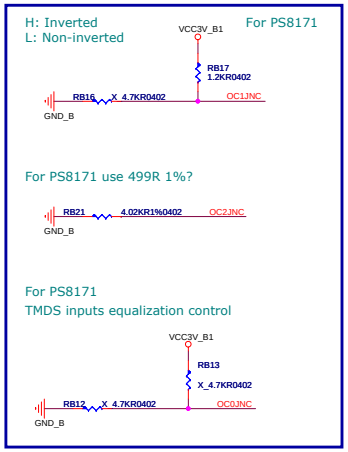
02/23 Change to 8 vias for EMI sugesstion

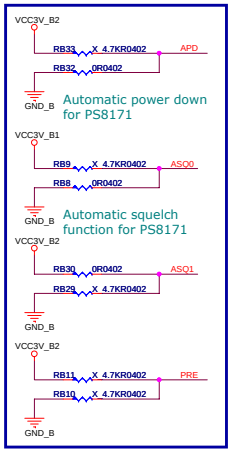
03/24 Remove LABB1

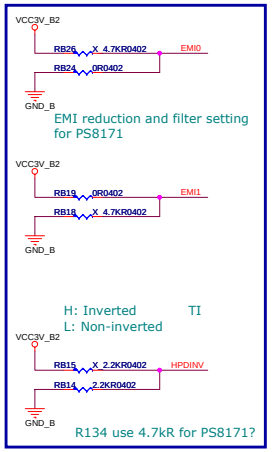




04/30 Change RIB7,RIB8,RIB9,CB23 from R11-0181012-W08 to R11-0331012-W08 and stuff on for EMI suggestion







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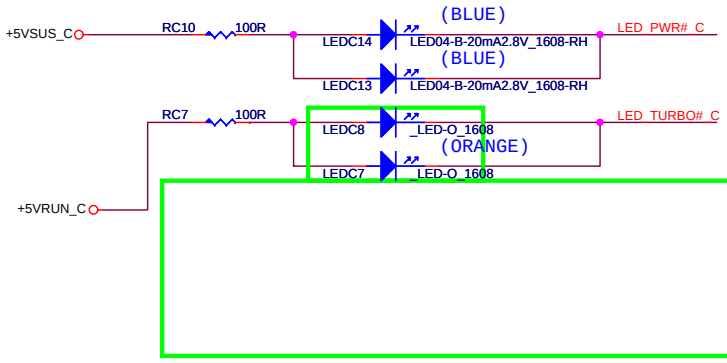
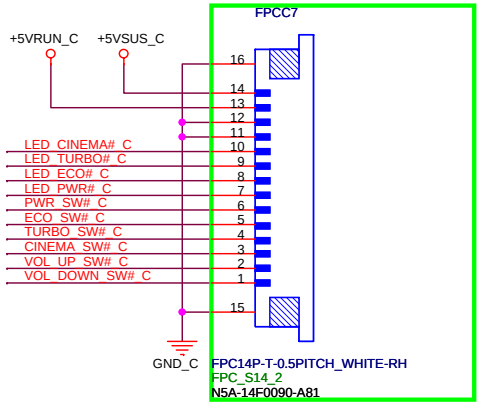
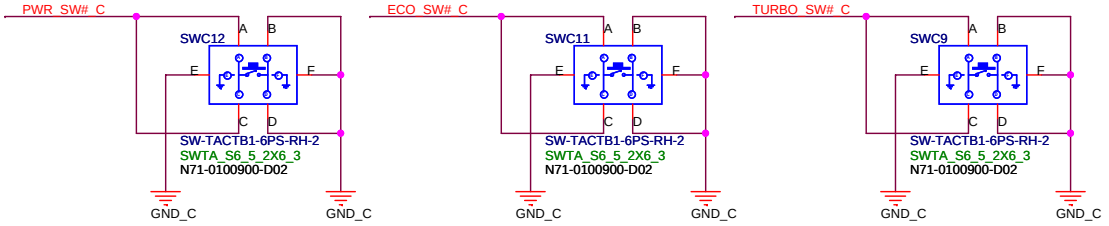


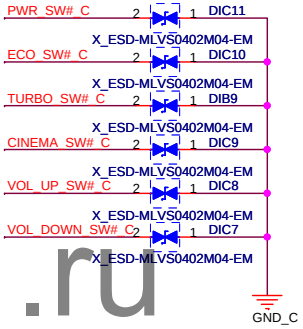
03/30 Change LEDC7.LEDC8 from D0C-04018F0-L05 to D0C-0400600-E07

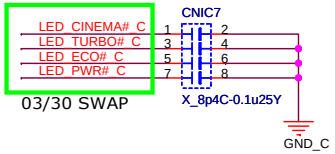
03/29 Remove ECO and Cinema LED for ID requestion



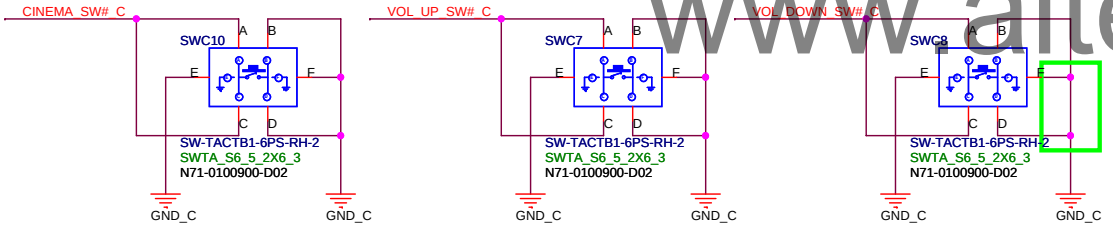
04/23 Change FPCC7 from N5A-14F0070-A81 to N5A-14F0090-A81(P/N only) for ME request



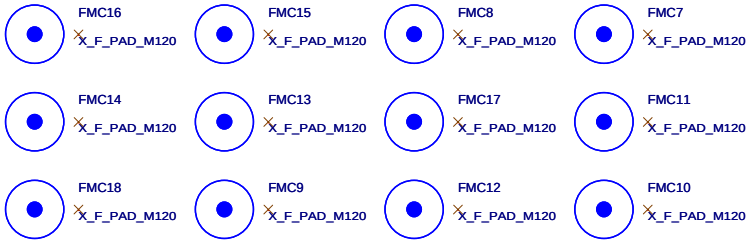


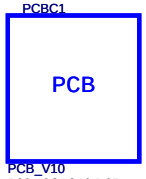


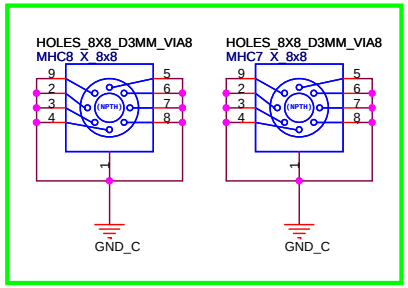
03/30 SWAP



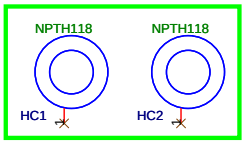
04/28 Fix SWC8's HW mismatch







02/10 Add 8 vias for EMI sugesstion



03/26 Add ME

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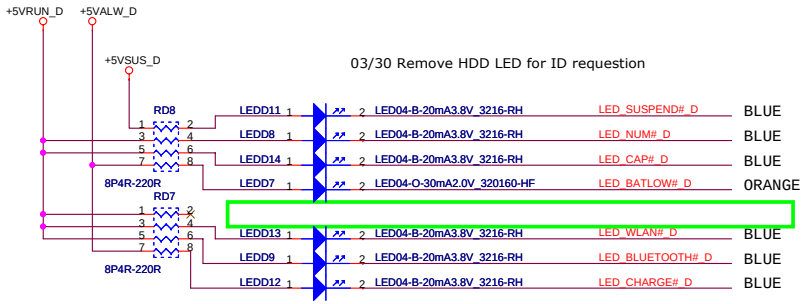

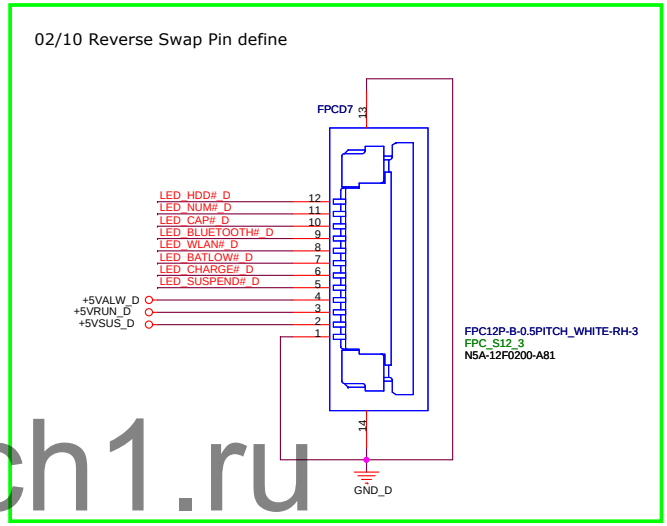

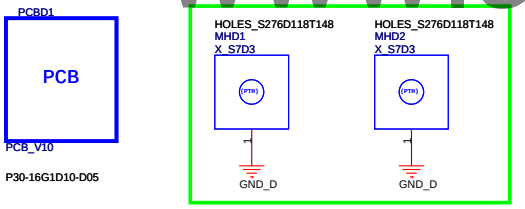

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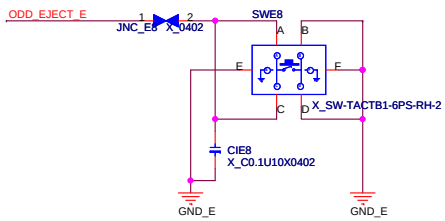
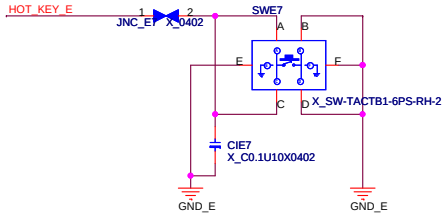
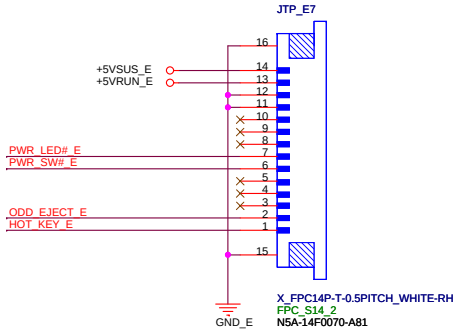
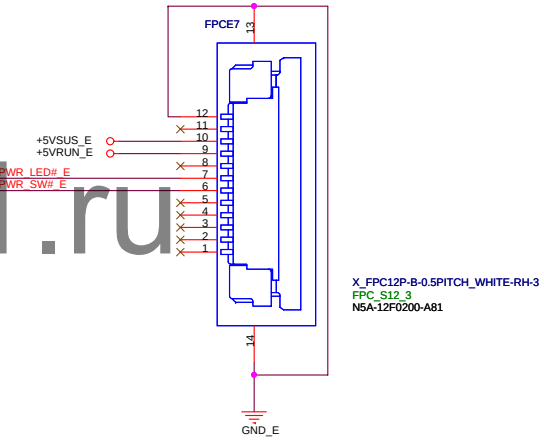
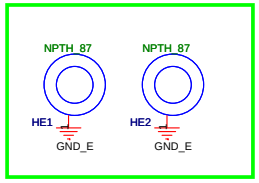




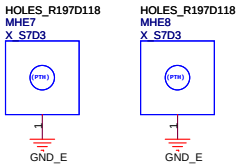






04/30 Add HE1,HE2 for ME requestion

P30-16G1E10-D05



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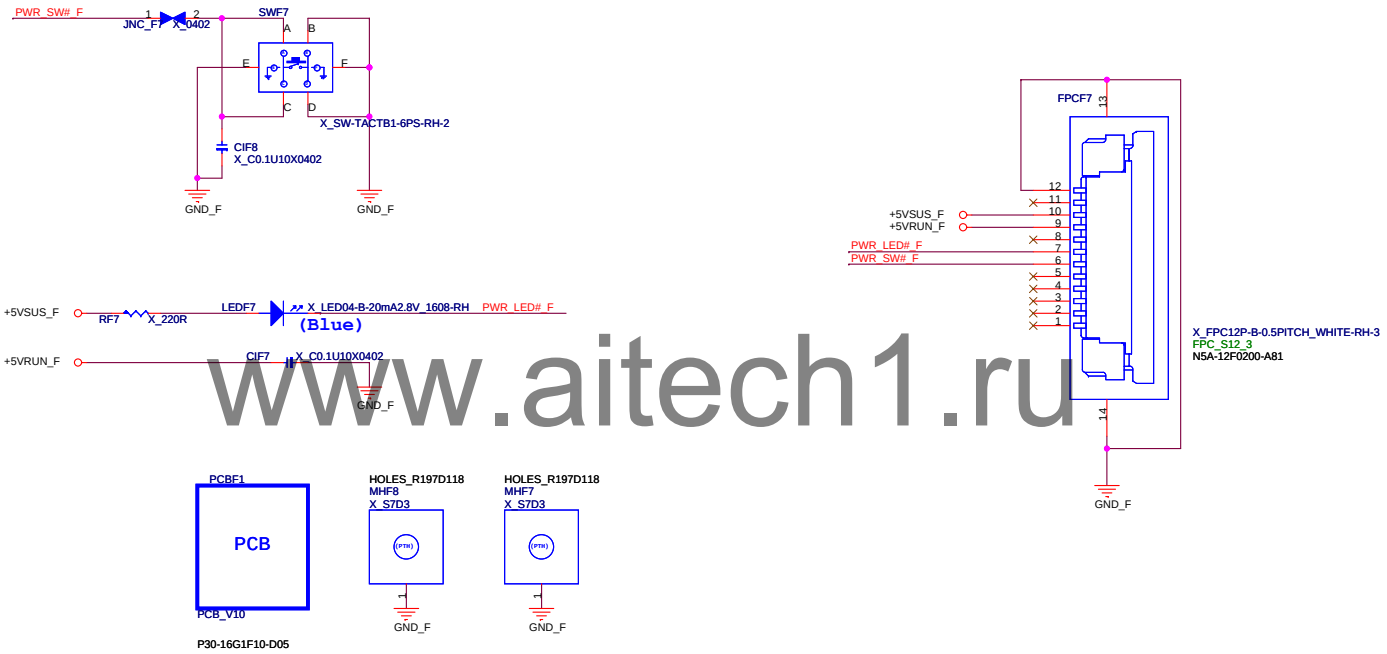

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0.A

2010/03/04 Change D21.D23 to D0C-04018F0-L05 and footprint change to LEDS_19_21SYGC

2010/03/19 Change R123 to 40.2R 1% for N11P-GV1 spec.
Change R63.R75 to 40.2KR 1% for N11P-GV1 spec.
Change U21 to UB6250
Change R239 to NC for UB6250
Change PR67 to 4.22KR 1% for Power requestion
Change PR65 to 2KR 1% for Optimus function stable
Change PC12 to stuff for Power requestion
HDMI_D2N_B and HDMI_D2P_B swap

0.B

2010/03/23 Change C346.C376 to 10uF and stuff
Change C347.C375 to stuff
Add R443 for FSA pull high resister
Move LID# pull high resister R444 to Main board
Change R166.R165 stuff states for mute AMP pop noise
Add C555.C556 for system stable
Change CA39 to 330pF and stuff for EMI sugesstion
Change LA10.LB13.LB14 to stuff for EMI sugesstion
Keyboard pin define swap

2010/03/24 Change C65.C68.C80.C443.R76 to NC
Copy BIOS1 info. to SPI_SOCK7 and remove BIOS1
Remove HDMI_V and LABB1
Change RA18 to NC
Change CHOKEA7 to 4.7uH
Change C346.C347.C375.C376 to NC
Change R221 to 1KR

2010/03/25 Change PC117 to C11-1011512-W08 for SMT cost down
Change CI21.CI22 to C11-1012012-W08 for SMT cost down
Change C502.C503.C504.C505.CB36 to C11-1022032-Y01 for SMT cost down
Change C11.C29.C394 to C11-1032082-W08 for SMT cost down
Change C16.C30.C31 to C11-1032082-W08 for SMT cost down
Change PC16.PC27 to C11-1042813-W08 for SMT cost down
Change PC61.PC71.PC78.PC102.PC127 to C11-1043612-W08 for SMT cost down
Change C7.C335.CA47.CA48 to C11-1043062-W08 for SMT cost down
Change PC17.PC18.PC19 to C11-1047512-T34 for SMT cost down
Change C24.C192.C218.C222.C416.C452.C479.C481 to C11-1042042-W08 for SMT cost down
Change C442 to C11-1053312-W08 for SMT cost down
Change CB39 to C11-1057613-T34 for SMT cost down
Change C308.C322 from C11-1067313-T04 to C11-1067014-T04 for SMT cost down
Change C12.C337.C402.C431 from C11-1067314-T34 to C11-1067014-T04 for SMT cost down
Change C95.C109 from C11-106A334-S02 to C11-1067014-T04 for SMT cost down
Change C38.C166 from C11-2242033-S02 to C11-2242013-W08 for SMT cost down
Change C200.C202 from C11-2253013-Y01 to C11-2253413-W08 for SMT cost down
Change CA12.CB22 from C11-2253014-W08 to C11-2253413-W08 for SMT cost down
Change C287.C298.C301 from C11-2257423-T34 to C11-2253413-W08 for SMT cost down
Change C8 from C11-2263027-W08 to C11-2267014-M09 for SMT cost down
Change C99.C121 from C11-2267334-A15 to C11-2267014-M09 for SMT cost down
Change C19.PC62.PC63 from C11-2267367-M09 to C11-2267014-M09 for SMT cost down
Change PC33 from C11-4712522-W08 to C11-4712012-W08 for SMT cost down
Change C537 from C11-4732012-W08 to C11-4732412-W08 for SMT cost down
Change PC45 from C11-4757014-W08 to C11-4757013-M09 for SMT cost down
Change CA46.CA49 from C11-4757313-W08 to C11-4757013-M09 for SMT cost down
Change C237.C238.C277.C278.C279.C281 from C11-4757434-T34 to C11-4757013-M09 for SMT cost down
Remove Power Gap G7.G8.G9.G10.G11.G13.G14
Change QB8 from D03-352AP09-F01 to D03-0640219-I08 for SMT cost down
Change Q24 from D03-352AP09-F01 to D03-0640219-I08 for SMT cost down

0.B

2010/03/25 Change D7 and D8 from D01-RB551V0-R06 to D01-BAS4000-W01 for SMT cost down
Change PR24 from R11-0101012-W08 to R11-0101033-Y01 for SMT cost down
Change R91 from R11-0103033-Y01 to R11-0103012-Y01 for SMT cost down
Change R164,R167,R168,R169 from R11-0104043-W08 to R11-0104042-W08 for SMT cost down
Change RA25 from R11-0153052-W08 to R11-0153T12-W08 for SMT cost down
Change RB45 and RB46 from R11-0202012-W08 to R11-0202T12-W08 for SMT cost down
Change R331 from R11-0560012-C36 to R11-0560T12-W08 for SMT cost down
Change R335 from R11-0822T12-Y01 to R11-0822012-R01 for SMT cost down
Change R345 from R11-0822T13-Y01 to R11-0822012-R01 for SMT cost down
Move ODM LED Function from B Daughter Board to MB

2010/03/26 Add ME
Change R428,R410,R402,R320,R322,R41,R39,R30,R90,R307,R238,R401,RB23
Footprint from 0R0402 to NC_0402_6 for cost down
ADD SB Heatsink and Screw x2

2010/03/29 Add ECO LED for Medion
Add CA56~CA58 for EMI Suggestion
Remove ECO and Cinema LED for ID requestion

2010/03/30 Change MHA8 to HOLES236D118_P
Add MHD1 and MHD2 for ME requestion
Change D21 from D0C-0403000-E07 to D0C-0400600-E07
Change LEDC7.LEDC8 from D0C-04018F0-L05 to D0C-0400600-E07
Add R446.R447.R448.LED27.LED28.LED29 for ME requestion
Remove HDD LED for ID requestion
Add SCREW3.SCREW4 for ME requestion

2010/03/31 Change PR61 from R11-3651T12-C36 to R11-0222T12-W08 for Power requestion
Change PR85 from R11-0593T12-Y01 to R11-6342T12-W08 for Power requestion
Change PR84 from R11-1212T12-Y01 to R11-7871T12-W08 for Power requestion
Change PR83 from R11-2551T12-W08 to R11-0332T12-W08 for Power requestion
Change PR103.PR104 from R11-0142T12-W08 to R11-1821T12-W08 for Power requestion

2010/04/02 Change PC96 from 0.047u to 0.068u for Power requestion
Change PR86 from 7.15KR1%0402 to 4.7KR1%0402 for Power requestion

2010/04/08 Change C347 and C375 to stuff for SA debug

1.0

2010/04/23 Add MYLAR2,MYLAR3,MYLAR4,MYLAR5 for ME request
Change PEC16 from C98-4712520-S03 to C98-4712540-P01 for SMT smooth
Change FPCC7 from N5A-14F0070-A81 to N5A-14F0090-A81(P/N only) for ME request

2010/04/27 Remove R163
Fix incorrect circuit @ P35
Add R449.Q33.Q34.+3V_SPDIF for SPDIF LED issue
Change QB8 from D03-0640219-I08 to D03-352AP09-F01 for SPDIF LED issue
Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

2010/04/28 Change CONN7 to NC for MVT
Change Q20.S1 input from PD# to EAPD for HP POP noise solution
Change R449 from 10kOhm to 100kOhm
Change Q21.S1 input from CODEC_HDA_RST# to EC_MUTE# for HP POP noise solution

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2010/04/28 Add R451
Add R450 for HP POP noise solution
Add RB49 for HP POP noise solution
Change R184 to NC for ACPI POP noise issue and Realtek suggestion
Change Q21.S1 input from CODEC_HDA_RST# to EC_MUTE# for HP POP noise solution
Change Q20.S1 input from PD# to EAPD for HP POP noise solution
Change R175.R174.Q21 to NC for HP POP noise sulotion
Change Q20,Q21 from BSS138 to 2N7002
Change R449 from 10kOhm to 100kOhm
Change C495 from C11-1067038-T34 to C11-1053054-W08
Change R170 from 100kOhm to 33kOhm
Fix SWC8's HW mismatch

2010/04/29 Remove R449.Q33.Q34.+3V_SPDIF

2010/04/30 Change RI15,CI18 to stuff for EMI suggestion
Change CI18 from C11-1022012-M09 to C11-4712012-W08 for EMI suggestion
Add CI60,CI60,CI62,CI63,CI64 for EMI suggestion
Change CI12,CI13,CI9 from to C11-1001012-W08 and stuff on for EMI suggestion
Change RIB7,RIB8,RIB9,CB23 from R11-0181012-W08 to R11-0331012-W08 and stuff on for EMI suggestion
Add HE1,HE2 for ME requestion

2010/05/03 Add UME3 and MYLAR6
Change RB49 from 750Ohm to 470Ohm

2010/05/04 Change PR10,PR41,PR141,PC8,PC50,PC131 to stuff for Power requestion

2010/05/11 Change PR59 from 10.7K to 11.3K for system stable

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